A Novel Step-Up Multilevel Inverter

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Abstract- Switched-capacitors based multilevel inverters are of two types: single-stage and two-stage. Two-stage topologies require four polarity-reversing switches of high blocking-voltage. A single-stage topology is proposed in this work which can synthesize thirteen levels with a single input source and three capacitors, with an overall voltage gain of three. The proposed inverter uses fourteen power switches, of which the blocking-voltage of ten switches are restricted to the source voltage. The remaining four switches have blocking-voltage equal to twice the source voltage and they operate at low frequency. Thus, for all switches, the blocking-voltage is less than the peak output voltage. The proposed module is validated experimentally and results are presented in this paper. A comparison of the proposed topology with other similar topologies is also presented.

Indexed Terms- Multilevel inverter, switched-capacitors, blocking-voltage

I. INTRODUCTION

RELIANCE on conventional fuels for energy needs of the world is being actively reduced due to concerns over pollution and price fluctuations [1]. As a result, vehicular electrification is being promoted and electric vehicles (EVs), hybrid cars, fuel cell vehicles etc. are penetrating the automobile market. Similarly, electric power production by using photovoltaic (PV) source is gaining significant grounds. For EV and PV applications, the input power source is of low dc voltage and the output ac waveform is required to fulfill stringent norms in terms of waveform quality. Switched-capacitors based multilevel inverters (SCMLIs) have been introduced to obtain a high quality stepped-up multilevel ac waveform from a dc source of lesser voltage [2]. MLIs also offer other benefits too such as: blocking-voltage of power switches is less (as compared to the magnitude of the output, generally referred to as the 'operating voltage'), reduced filtering requirements, much reduced dv/dt variation experienced by the load etc. [3]. SCMLIs enable the voltage-gain to be greater than unity with the use of switched capacitors [4,5]. Numerous SCMLI topologies have recently proposed [2-15]. The SCMLI modules presented in [2, 7, 9, 12] feature self-balanced capacitors but have high component count, while the SCMLI structures discussed in [3, 6, 10, 11] require power switches with high blocking-voltage capability. The topology presented in [14] requires a complex closed loop control scheme to balance the capacitor voltage. The topology presented in [5] is a two-stage structure with H-bridge switches having large blocking-voltage requirements. In this work, a single stage SCMLI topology is presented with following features: (a) voltage gain per module is three; (b) thirteen-level waveform is generated using one dc source, three capacitors and fourteen power switches, with no requirement of additional diodes; (c) all capacitors are self-balanced; (d) blocking-voltages of all power switches are significantly less than the operating voltage; and (e) the two power switches with clocking-voltage equal to two-times the input voltage, can be operated at line frequency, thereby minimizing the switching losses. The remaining paper is as follows: the proposed topology is explained in section II, along with a comparison with other topologies. A switching methodology is discussed in section III. Experimental results are presented in section IV for validation, while conclusions are discussed in section V.

II. PROPOSED THIRTEEN-LEVEL INVERTER

The structure of the proposed thirteen-level inverter is shown in Fig. 1 and it consists of fourteen power switches S_j {j = 1 to 14}, three capacitors (C_1, C_2 and C_3) and one dc source (V_{dc}). The output ac voltage is marked as '$v_{ac}(t)$'. Voltage of capacitor C_1 is to be maintained at V_{dc}, while voltages of capacitors C_2 and C_3 are to be maintained at $0.5V_{dc}$ each.

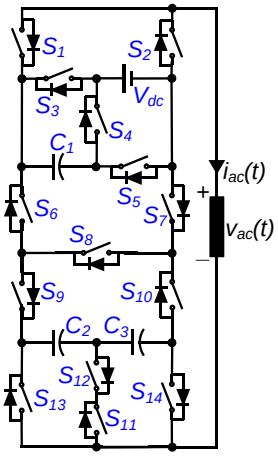


Fig.1. Proposed 3X-voltage-gain 13-level switched capacitor inverter

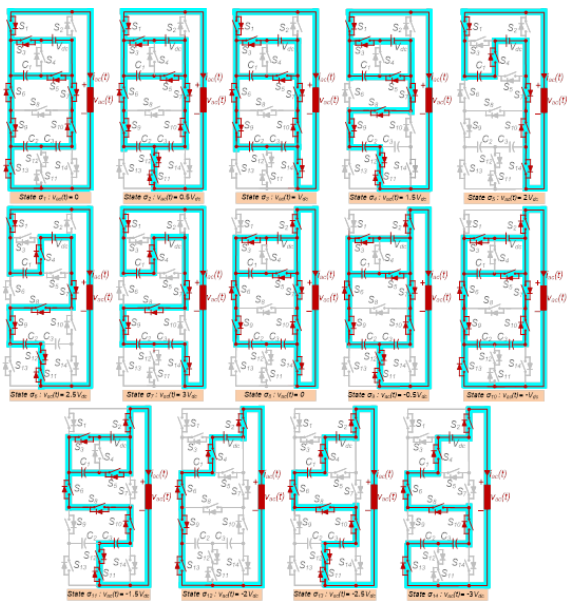


Fig.2. Working states for the proposed thirteen-level inverter with switched capacitors

For the proposed inverter, the blocking-voltage requirements for the power switches are shown in Table I.

TABLE I

BLOCKING-VOLTAGE OF POWER SWITCHES IN THE PROPOSED INVERTER WITH V_{DC} AS INPUT VOLTAGE AND $3V_{DC}$ AS PEAK OUTPUT

Blocking Voltage	Power Switches
0.5 V_{dc}	S_{11}, S_{12}
V_{dc}	S_3, S_4, S_5, S_8, S_9, S_{10}, S_{13}, S_{14}
$2V_{dc}$	S_1, S_2, S_6, S_7

All the valid operating states σ_j {j = 1 to 14} for the proposed inverter are summarized in Fig.2. In states σ_1, σ_2, σ_3, σ_4, σ_8, σ_9, σ_{10} and σ_{11}, C_1 comes in parallel with V_{dc} and keep it self-balanced. Similarly, C_2 and C_3 combined come in parallel with V_{dc} during the states σ_1, σ_2, σ_3, σ_8, σ_9 and σ_{10}. It can be seen that both the states σ_1 and σ_8 synthesize zero voltage at the output terminals. A judicious use of states can help in operating the switches S_1 and S_2 at a frequency equal to the line frequency. For this, zero voltage levels in the positive and negative halves should be obtained by using states σ_1 and σ_8 respectively. A procedure to attain the same is described in section III.

As far as the classical multilevel topologies (viz. diode-clamped, flying capacitors and cascaded H-bridge) are concerned, the voltage gain is unity, whereas, the switched capacitors-based structures offer a voltage gain greater than unity. Hence, an appropriate comparison of the proposed topology would be with other switched capacitors-based structures. In Table II, a comparison of the proposed inverter with other SCMLIs is presented considering the requirement of components. In Table III, the comparison is extended with the consideration of blocking-voltage (BV) and total-blocking-voltage (TBV) requirements, as these factors greatly determine the cost and application of the topologies [17,18]. Since the topologies being considered for comparison have different number of levels in the output, the number of components per output level is also shown Table II in its ninth column and it can be observed that the proposed inverter requires minimal components per level. It can also be observed from Table II and Table III that topologies presented in [3, 6, 7, 10, 11] require power switches with large BVs, whereas the TBV is significantly high for the topologies presented in [5, 6, 7, 11, 12]. It should also be noted that the proposed topology is highly competent in terms of the total standing voltage and overall component count of 3.384 per level. Though topology presented in [16] is more advantageous in terms of TBV and BV, it requires more components as compared to the proposed module.

TABLE II

COMPARISON OF THE PROPOSED TOPOLOGY WITH OTHER SWITCHED CAPACITORS BASED TOPOLOGIES (N_L = NUMBER OF OUTPUT LEVELS, N_{IS} = NUMBER OF INPUT SOURCES, N_S = NUMBER OF POWER SWITCHES, N_D = NUMBER OF MAIN DIODES, N_{AD} = NUMBER OF AUXILIARY DIODES, N_{GD} = NUMBER OF GATE DRIVERS, N_C = NUMBER OF CAPACITORS)

Reference	N_L	N_{IS}	N_S	N_D	N_{AD}	N_{GD}	N_C	Component count per level
[2]	5	1	9	9	0	9	1	5.600
[3]	9	1	10	10	1	8	2	3.444
[4]	9	1	12	12	0	11	2	4.111
[5]	7	1	10	10	0	10	2	4.571
[6]	5	1	6	6	2	6	1	4.200
[7]	7	1	16	16	0	14	2	6.857
[8]	5	1	6	6	2	6	2	4.400
[9]	5	1	9	9	1	8	1	5.600
[10]	5	1	6	6	1	6	1	5.000
[11]	5	2	8	8	0	8	0	4.800
[12]	5	1	12	12	0	12	2	7.600
[13]	5	1	7	7	3	7	2	5.200
[16]	9	1	11	11	0	10	2	3.777
Proposed	13	1	14	14	0	13	3	3.384

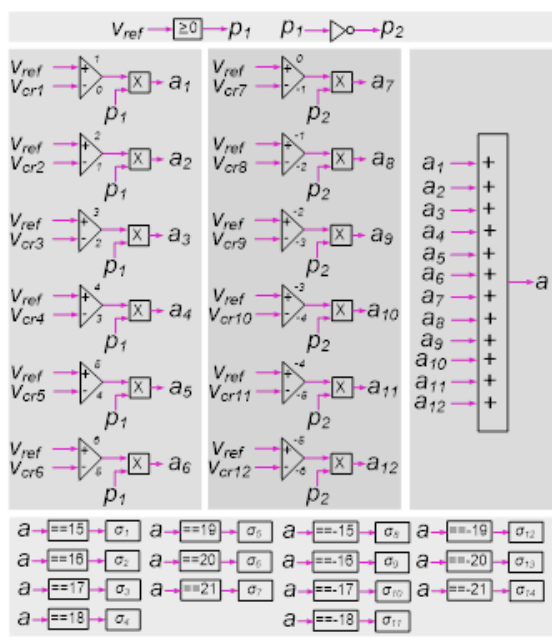
TABLE III

COMPARISON OF THE PROPOSED TOPOLOGY WITH OTHER SWITCHED CAPACITORS TOPOLOGIES IN TERMS OF TOTAL BLOCKING VOLTAGE (TBV) AND BLOCKING VOLTAGE (BV) REQUIREMENTS FOR AN INPUT DC VOLTAGE V_{IN}

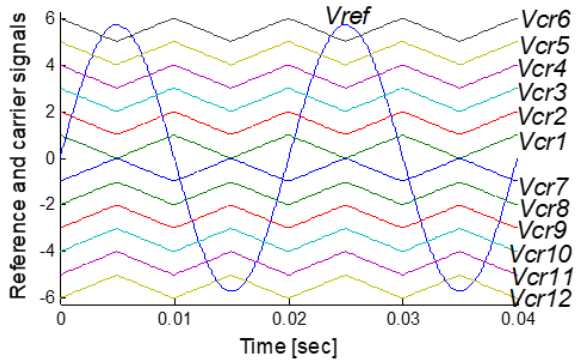
Reference	N_L	TBV	BV	TBV per level in *per unit* w.r.t. V_{in}	BV per level in *per unit* w.r.t. V_{in}
[2]	5	$9V_{in}$	V_{in}	1.800	0.200
[3]	5	$11V_{in}$	$2V_{in}$	2.200	2.200
[4]	9	$11V_{in}$	V_{in}	1.222	0.111
[5]	7	$18V_{in}$	$3V_{in}$	2.571	0.428
[6]	5	$12V_{in}$	$2V_{in}$	2.400	0.400
[7]	7	$16V_{in}$	$2V_{in}$	2.285	0.285
[8]	5	$8V_{in}$	V_{in}	1.600	0.200
[9]	5	$9V_{in}$	V_{in}	1.800	0.200
[10]	5	$11V_{in}$	$2V_{in}$	2.200	0.400
[11]	5	$12V_{in}$	$2V_{in}$	2.400	0.400
[12]	5	$20V_{in}$	V_{in}	4.000	0.200
[13]	5	$9V_{in}$	V_{in}	1.800	0.200
[16]	9	$10V_{in}$	V_{in}	1.111	0.111
Proposed	13	$17V_{in}$	$2V_{in}$	1.307	0.153

III. SWITCHING METHODOLOGY

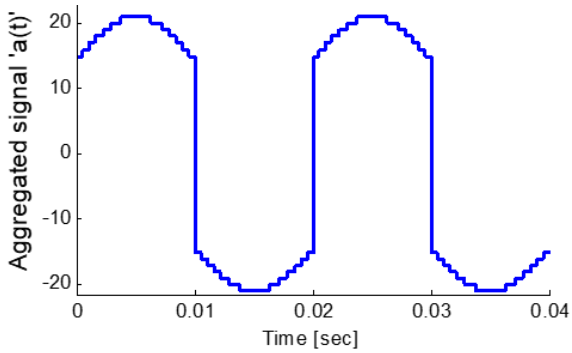
While the proposed topology can be modulated with any of the schemes for multilevel inverters with suitable adaptation, the multicarrier PWM scheme as described in [19] is used in this work as it felicitates the utilization of both the zero states. The scheme is shown in Fig. 3(a). Twelve triangular waveforms V_{crj} {j = 1 to 12} of 100Hz frequency each are used as carriers and are configured in phase opposition disposition. A sinusoidal waveform V_{ref} of 50 Hz frequency is taken as the reference signal. These reference and carrier signals are shown in Fig. 3(b). A continuous comparison of the reference with the carriers is carried out. If the reference V_{ref} is greater than carriers, the comparators give 1, 2, 3, 4, 5, 6, 0, -1, -2, -3, -4 and -5 respectively for carriers V_{crj} {j = 1 to 12}. On the other hand, if the reference V_{ref} is less than carriers, then comparators give respective outputs as 0,1,2,3,4,5,-1,-2,-3,-4,-5 and -6. Signals a_j {j = 1 to 12} are added so as to obtain an aggregated signal 'a', shown in Fig. 3(c).



(a)



(b)



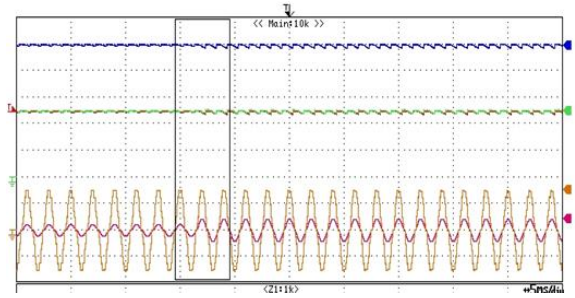
(c)

Fig.3. (a) switching scheme for the proposed module; (b) reference and carrier signals; and (c) aggregated signal 'a'

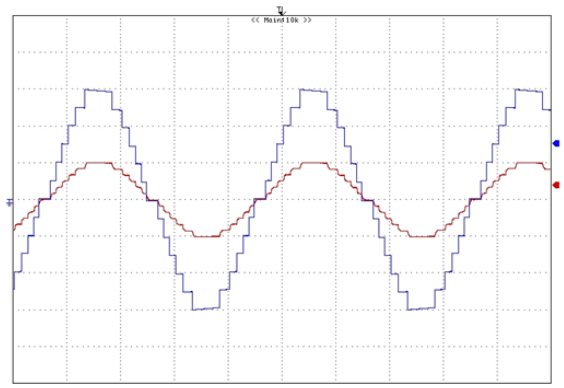
Aggregated signal '*a*' has seven positive levels from 15 to 21 in steps of 1 and seven negative levels from -15 to -21 in steps of -1. A one-to-one relationship of these levels in the output waveform is utilized to extract switching pulses (for the specific working states) as shown in Fig. 3(a).

IV. EXPERIMENTAL VERIFICATION

To validate the proposed topology, a laboratory set-up was made using discrete power switch modules (with MOSFETs IRF460 with suitable gate drivers). The input voltage was set to 100V and three capacitors of 2200μF each were used as C_1, C_2 and C_3. dSPACE DS1103 was used to generate real time gate signals. Carrier signals of 100 Hz and reference signal of 50 Hz was used with a modulation index of 0.95. The experimental waveforms are shown in Fig. 4 for an inductive load. The capacitors C_1, C_2 and C_3 are self-balanced at their respective voltages of 100V, 50V and 50V, even when the load current is doubled. The output waveform is a thirteen-level waveform in steps of 50V as expected. Thus, validity of the proposed structure is confirmed in terms of its working and capability of capacitors to be self-balanced.



(a)



(b)

Fig.4. Experimental results: (a) Voltages of capacitors C_1, C_2 and C_3, load voltage and load current; and (b) zoomed waveforms of load voltage and load current

CONCLUSION

A thirteen-level inverter with three-time voltage boosting capability is presented in this paper. The switched capacitors used in the topology are self-balanced and the PIV of all the power switches are significantly less as compared to the operating voltage. A comparative study of the proposed topology with the contemporary topologies indicates its merit in terms of component count and total standing voltage. Experimental results validate the proposed structure. The proposed module can be used for applications which involve low voltage dc sources as input while requiring a high-resolution ac waveform with increased voltage as output.

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