A Review on Dynamic CMOS Logic Noise Tolerant Techniques

ANKUL GAUTAM[1], DURGESH KUMAR[2]
[1,2] *Department of Electronics And Communication Engineering, Poornima College of Engineering, Jaipur, Rajasthan*

Abstract ***Dynamic logic vogue is principally used for top fan in and high-performance circuits thanks to its smaller space and quick superior speed. This vogue comes with a retardant of low noise margin that makes it a lot of liable to noise than static CMOS circuits. It conjointly faces some charge sharing and escape issues. A little quantity of noise at the input will cause associate degree undesirable modification at the output. Domino logic (dynamic logic with associate degree electrical converter at the output) cojointly faces this drawback. This paper consists of an summary of assorted noise tolerant techniques for dynamic logic explaining their functioning and responsible ness for compacting noise.***

Indexed Terms - Delay, Technology, Scaling, Threshold, voltage, Power consumption, Noise ,Immunity, Leakage tolerance ,Diode flat- footed domino

I. INTRODUCTION

Technology scaling has created some way for incorporating additional and additional transistors on one chip and has improved the performance of VLSI systems. Technology scaling has return up with several problems in deep submicron (DSM) Styles. Noise immunity is extremely necessary concern in DSM. The increasing leak currents, gaint method variations, high clock frequencies, noise and lots of different DSM noise sources all contribute in degradation of noise immunity.[1]As the technology scaling happens provide voltage must be scaled right down to maintain device dependability that successively demands for reduced threshold voltage . Reduction in threshold voltage decreases the noise immunity because it ends up in exponential increase in sub threshold leak currents that successively will increase sub threshold leak power.

Fig.1 shows generalized CMOS dynamic logic circuit . Here the operating of dynamic gates happens thanks to the fugitive charge storage within the dynamic nodes . For its operating correct and continuous up gradation of internal nodes is needed. This puts forward a vital factor that charge refreshing is done by the appliances of standard and periodic clock signal within the figure given higher than a dynamic logic circuit is given that tells north American country that this system helps in reduction. Of variety of transistors used and thence intrinsically any logic perform is enforced with dynamic logic .Almost all the dynamic cicuits are supported 1st precharging the output node so evaluating the output level in line with the applied inputs.

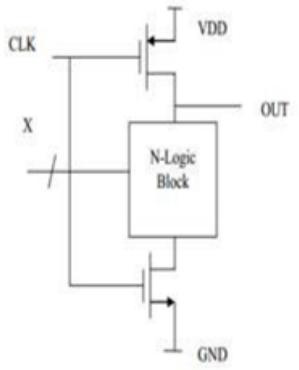

Fig.1: Dynamic logic circuit[2]

The precharge part is for setting the circuit at a predefined initial state whereas the particular logic response is set through out the analysis part. Since dynamic logic provides terribly low shift threshold voltages they are prone to numerous style and method variations.

II. LITERATURE SURVEY

According to the paper by Misbah Manzoor, Shekhar Verma , Mahwash Manzoor,they describes the different types of noise tolerant techniques in dynamic

logic. In which we learn the noise effect on the various effects.[2] According to the paper by Rajneesh sharma and shekhar verma, they describes the comparative analysis of static and dynamic cmos logic design.effect of voltage variation on power and delay of static and dynamic cmos logic styles studied.[3]

III. NUMEROUS NOISE TOLERANT DYNAMIC TECHNIQUES

Noise in VLSI circuit systems could also be considered any amendment that changes and takes the dynamic node voltages from their actual voltage. Noise has nice impact on the performance of assorted circuits that embody power provide variations, crosstalk, leak etc. Noise sources in dynamic logic circuits are broadly speaking classified into 2 types :1) Gate internal noises together with charge sharing noise, leak noise, then on and 2)external noises ,together with input noise ,power and background signal , and substrate noise[4].From past few decades numerous techniques to enhance the noise immunity of Dynamic CMOS logic gates are developed they are categorized as

1) Mistreatment keeper
2) Raising supply voltage
3) Precharging internal nodes
4) Diode web footed domino
5) Dynamic feed through logic

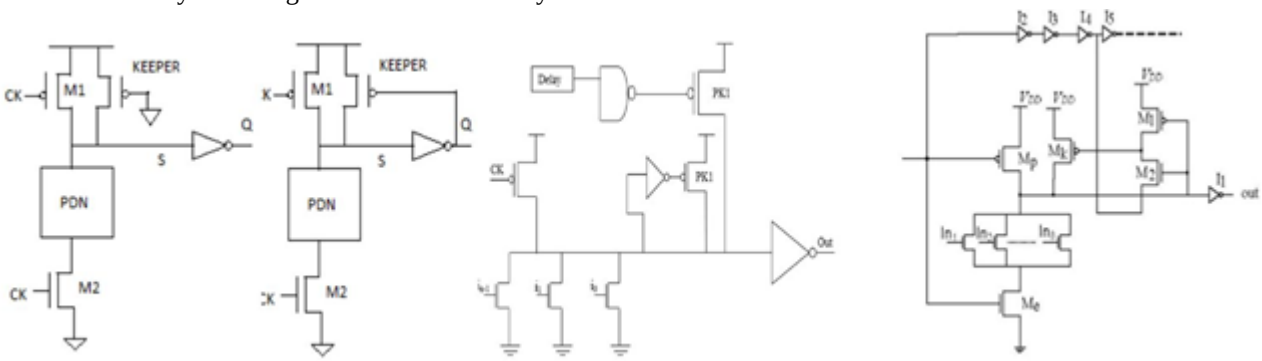

Fig2: Improving noise immunity of dynamic logic gates using (a) Always-on keeper. (b) Feedback keeper. (c) Conditional keeper.(d) Saturated keeper[2]

A. Using keeper

One of the terribly normally used technique to extend noise immunity is to use keeper numerous kinds of keepers square measure used that square measure given as beneath ,the essential perform of keeper is to provide little current from power supply therefore on keep charge keep in dynamic node as shown in figure2(a), the gate is typically tied to ground this is often known as invariably on keeper however it expose the matter of dc power consumption problem[4].In order to avoid this drawback the feedback keepers were employed in that the output was given as a feedback to the keeper that shown in figure2(b).It reduced the dc power consumption drawback baby – faced earlier any the actual fact was determined that the utilization of keeper causes a competition drawback that the size of the keeper conjointly matters the scale of keeper semiconductor unit is unbroken smaller the associate degree a transistors in a very pull down network to scale back delay and power consumption except for higher noise immunity its size is unbroken massive therefore size of keeper sometimes provides exchange for noise reduction with different parameters therefore conditional keeper was used as shown in figure2(c)that consist of 2 keepers . This system leads to less discharge and quicker analysis. Here one

amongst the keeper pk1 is unbroken massive and is deployed once some delay to stop inaccurate discharge of dynamic node once all inputs square measure low. the little keeper pk2 remains on to complete charge discharge till pk1 is activated [1].Another keeper technique known as saturated keeper is employed figure 2(d). Here at the beginning of analysis part the keeper is biased in saturation region to scale back delay and power and providing desired noise margin to succeed in this goal the gate voltage of keeper is unbroken at VDD-VT level. The gate voltage of the keeper, the signal that controls the driving current of

keeper is connected to the output of a Not gate with input sensing the dynamic node voltage. At the start of analysis part clock and square measure high, if the input vectors don't need discharging the dynamic node the gate voltage of keeper are going to be maintained at VDD-VTn2 and can give desired noise immunity [5].

B. Raising supply Voltage

1) D'Souza's methodology

Figure 3(a) shows two input sodium ND gate victimization D'Souza's methodology. The semiconductor unit Mn shown in figure is turned on within the measure part and it brings down node N1 that as a result activates Mp and therefore forming potential divider. Voltage at N1 depends on sizes of Mp and Mn. Since N1 is supply node of semiconductor unit MB, the increased N1 voltage raises threshold voltage of MB as a result of frame y impact. The transistor | junction semiconductor unit MB activates only the difference between input voltage at B and also the N1 exceeds the raised threshold voltage of transistor. It provides higher noise immunity however it's an obstacle of dc power consumption and conjointly voltage swing isn't rail to rail .[6]

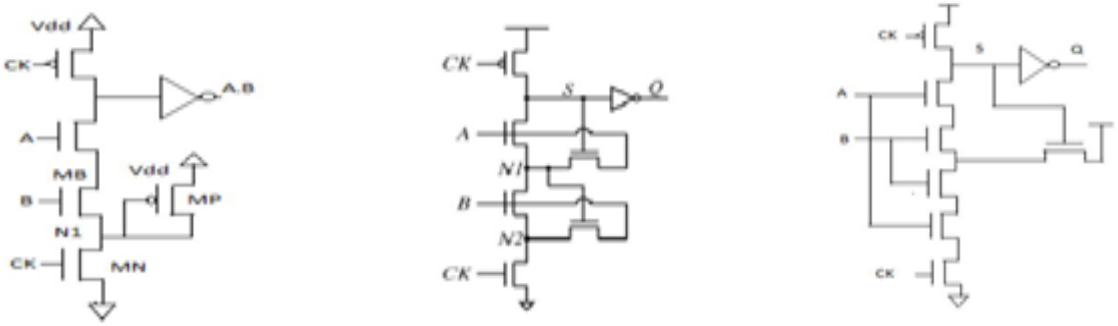

Fig3: Raising supply voltage. (a) D'Souza's method. (b) Mirror technique. (c) Twin transistor technique [2]

the noise tolerance. once the pull down network is off the mirror network is additionally off therefore pruning the dc conducting path. From the NMOS pull up junction semiconductor unit through bottom clock controlled transistor, therefore dc power consumption is resolved [4].However this system increases space and speed.

3) Twin Transistors Technique

Figure 3(c) shows two input NAND gate with twin semiconductor unit technique. this system conjointly gives noise immunity however at the cost of energy. Here extra semiconductor at every node is employed to precharge internal nodes. This technical schoolnique helps to resolve .charge sharing drawback

2) Mirror Technique

The mirror technique use impotence to 2 input NAND gate is shown in figure 3(b).It merely duplicates the pull down network and uses a feedback management NMOS semiconductor unit that decreases dc power consumption and will increase however the disadvantage of th is technique is that it will increase delay and node capacitance. [4]

C. Internal Node Precharging

1) Precharge all internal nodes

In case of complicated logic gates charge sharing happens between the inner nodes within the pull down n etwork and therefore the dynamic nodes which ends up in wrong gate shift. a straightforward thanks to avoid this is often to precharge the inner nodes within the pull down network in conjunction with precharging dynamic nodes. when all the inner nodes square measure precharged charge sharing is eliminated at the price of larger space and enhanced load capacitance on clock net[4]. This is often shown in figure 4(a).

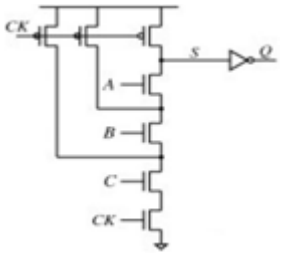

Fig. 4: (a) Precharging all internal nodes[2]

2) Convino's strategies

This technique implementation is shown in figure 4(b).This technique is largely a modification of internal node precharging. It provides additional noise immunity thanks to precharging PMOS the scale of PMOS electronic transistor will be accustomed change the shift threshold of dynamic computer circuit. the disadvantage of this method is it can't be applied to wide fan in or gates [6].

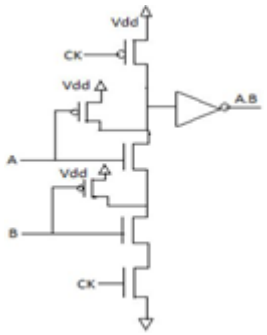

Fig4: (b) Convino's method[2]

D. Diode flat-footed Domino

This technique shows sensible improvement in noise immunity as compared to face and domino circuits. Here a NMOS electronic transistor is employed in diode configuration i.e. gate and drain terminals square measure tied along and square measure additional nonparallel with analysis network of domino circuits, here stacking impact greatly reduces noise by decreasing the run within the analysis path and thence will increase hardiness. chiefly comparators and multiplexers and used mistreatment this system. to extend the speed a current mirror is additionally employed in analysis network. this system is additional helpful for higher fan in gates [7].This is shown in figure 5.

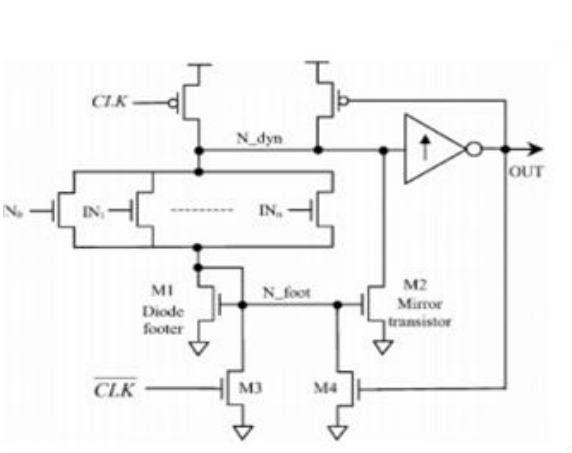

Fig5: Diode flat-footed Domino Logic [2]

Table I. Comparison of Dynamic Circuit Noise Tolerance Techniques [2]

Class	Technique	Dc Power Consumption	All Noises
A	Always on keeper	More	Effective for almost all noises
	Feedback keeper	Less	Effective for almost all noises
	Conditional keeper	More	Mostly good for gate internal noises
B	Saturated keeper	Less	Not effective for all noises
	D'Souza	More	Effective for almost all noises
	Mirror technique	Less	Effective for almost all noises
	Twin transistor	Less	Not effective for all noises
C	Precharging internal nodes	Less	Not effective for all noises
	Convino's method	More	Not effective for all noises

IV. CONCLUSION

Different noise tolerant techniques are mentioned in Table1. Keeper technique used is incredibly helpful in providing smart noise immunity and provides lesser power consumption additionally to lesser space as shown in Figure half dozen. It is most generally used technique and may be utilized in totally different forms like feedback keeper, conditional keeper etc. Raising the supply voltage techniques that embody mirror and twin semiconductor technique end in additional Si space of the circuit, low speed of circuit and redoubled power dissipation. Techniques like internal node precharging puts forward the matter of dc power consumption. it's effectively used for under specific styles of logics. Diode flat-footed Domino is generally used for top fan-in circuits and may be a escape tolerant and high performance technique. It gave higher results than conditional keeper technique which might seen within the table and graph given below. Diode flat-footed domino conjointly consumes less power.

REFERENCES

[1] M. Elgebaly and M. Sachdev, "A Leakage Tolerant Energy Efficient Wide Domino Circuit Technique," IEEE, 2002.

[2] Misbah manzoor, Shekhar verma, Mahwash manzoor,"Noise Tolerant Techniques In Dynamic CMOS Logic," IEEE 2015.

[3] Rajneesh sharma ,Shekhar verma "comparative analysis of Tatic and dynamic cmos logic design,"IEEE 2011

[4] L. Ding and P. Mazumder, "On Circuit Techniques to Improve Noise Immunity of CMOS Dynamic Logic,"IEEE Transactions on Very Large Scale Integration VLSI Systems, vol.12, no.9, September 2004.

[5] H. Mahmoodi and K. Roy, "Diode-Footed Domino: A Leakage-Tolerant High Fan-in Dynamic Circuit Design Style,"IEEE Transactions on Circuits and Systems, vol.51, no.3, March 2004.

[6] S.Booba and I.N.Hajj, "Design of Dynamic Circuits with Enhanced Noise Tolerance," IEEE, 1999.

[7] A.Amerabadi, A.Chechelcheraghi et al, "Low Power and High Performance Clock Delayed Domino Logic using Saturated Keeper," IEEE, 2006.