Output Voltage Regulation Of High Voltage Gain Non-Isolated DC-DC Boost Converter

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Abstract -This paper features a high voltage dc-dc boost converter based on the 3-state switching cell for divided clamped-inverters with neutral split-point. A study of the proposed converter is carried out taking into account the operation in continuous conduction mode and the duty cycle of overlapping mode is greater than 0.5. The key characteristics of topology are the high-frequency operation of the input inductor, whereas, for two times the frequency, the voltage pressure across the switch is lower than half the output voltage and naturally clamped by the one output Capacitor to minimize weight and volume, which enables MOSFET transistors with reduced intrusion ON-resistance to be used. The output voltage can be further enhanced by increasing the transformer turning ratio without compromising voltage stress across the switches; and the output voltage is of course balanced, making the converter ideal for supplying divided-up inverters. In the literature initially, several topologies where high voltage increases are possible are examined. To verify the theoretical study and demonstrate converter efficiency the theory of operation and experimental results for the 1-kW prototype were presented.

Index Terms- CCM, CCM-OM, DCM, VMC, NPC

I. INTRODUCTION

Several Low DC Voltage is frequently needed by battery's, solar panels, small turbines in the many types of applications such as Uninterruptible power supply (UPS) and adjustability drives. Typical low tension is 12 to 125 V and should be increased to 300 or 440 V to supply the dc-ac stage with a dc bus [1]. It is worth pointing out that in such applications the ordinary boost converter is inadequate because high output voltages need a high value for the duty cycle, which, on the other hand, leads to the main switch being switched on for long periods. As the current through the diode is more, the reverse recovery phenomenon is existing. A feasible solution would also be the attachment of several boost converters in the cascade, but increased complexity and reduced efficiency are existing [2]. Furthermore, due to high-order dynamics, flexibility is applied to the control system.

Many high-voltage topologies have been introduced in the literature and discussed in the following way, to address the above limitations. Conveniently designed to be low power and low input voltages, the standard push-pull converter is twice that of input [3] due to voltage tension over the main switches. Further disadvantages include the transformer leakage inductivity, which causes the high voltage peak through the switch during switching to switch turns, the consequent need to clamp the circuit to maintain switching, and potential transformer saturation because of its asymmetrical nature and possible variations in the main switch duty cycle.

A boost converter is presented in [4] with two inductors and an auxiliary transformer but the source and the load are not connected to the same reference node. A new structure version is implemented in [5], which now has the same reference node. Both converters use a unit turn ratio transformer, in which the load flows through two inductors that keep the current shared correctly. The output side is arranged as a double-rectifier to maximize the voltage gain. The main features of the proposal are the ripple input current, with the highest voltage of half of the output

voltage through switches and higher performance of 90 percent. It must be noted, however, that the converter requires isolated drive circuits to be used for switches or insulating the sample output voltage [4]. With the converter in [5], the entire charge current runs through the capacitors, thereby affecting robustness and reliability. In addition, the output voltage must be 4 times the input voltage at least, while the output capacitor should be charged before starting up. The eventual simultaneous turn-off for the main switches would, finally, lead to a severe breakdown as the inductors cannot be discharged, which would require an external safety circuit. The [6] and [7] topologies are focused on the utilization of switched Capacitors and also on the incrementing voltage. Since several Capacitors are required, this structure is limited to low-power applications with the high voltage stress of the active switches.

A multiplier capacitor interlaced boost converter is offered in [8] and [9]. This system is similar to the Capacitor series used in the primary inductor transducer with one end, which allows for an increased static gain. Although high-current applications with reduced input ripple current and voltage stress through main switches represent half the total output tension are recommended, the high current through the series of capacitors can result in significantly reduced efficiency in high-power applications. A generic cell is used for an interlaced boost converter in [10], where each boost inductor is connected to one more inductor. The proposal retains the same structure as the conventional two-phase dc-dc converter but adds two combined inductors, two diodes, and two Capacitors. High voltage gains are achieved when the incoming current is constant and voltages are less than half the output voltage through the switches. High efficiency and high-power density are present in topology, but the hard switching of active switches causes noticeable losses. The soft switching cells studied in [11] and [12] can be used to reduce them.

The interlaced boost converter is offered with a soft-switching cell in [12] where soft switching and a high voltage increase are obtained. However, there are two more resonant Capacitors, one resonant inductor, and two series diodes, with the main switch and an auxiliary switch, which are compounds of some complexity. In [2] it has been shown that various converters can be cascaded to increase the static gain by deriving quadratically and cubic converters. In [13] the work introduces a quadratic stimulus converter with a quasi-resonant cell to give soft switching. The major benefits are more static gain than the ordinary boost converter, soft switching, and high performance for a large load range. The semiconductor elements have the main problem with high current and voltage. The main disadvantages are linked to the high complexity due to a soft commutation by an external auxiliary switch.

In [14], the voltage gain can be further increased by a simple adjustment of the turn's ratio of a high-frequency transformer. The transformer is very simple. Through the whole load spectrum, high performance is achieved. The prototype is only 250 W and, as there is an increase in circulating energy due to the resonant tank, is not recommended for high-current high-power applications. Furthermore, the tension of voltage over the main switches corresponds to the voltage output. Since the 3SSC definition was first proposed in [15], various dc-dc and ac-dc converter topologies have been proposed for the last ten years in the literature. Let us focus the study explicitly on high-voltage 3SSC converters [16]. In [17], a new family of dc-dc converters was introduced, using the 3SSC and VMC (Voltage Multiplier Cells), while major progress was made in reducing voltage stress over the main switches, decreasing ripple input current, reducing the magnetic size and weight, reducing switching losses and achieving a high efficiency over the whole load-bearing range. However, the shortened service life and the high part count of series Capacitors can be indicated as disadvantages. Driving losses in the multiplier diodes are also of major concern when many VMCs are used.

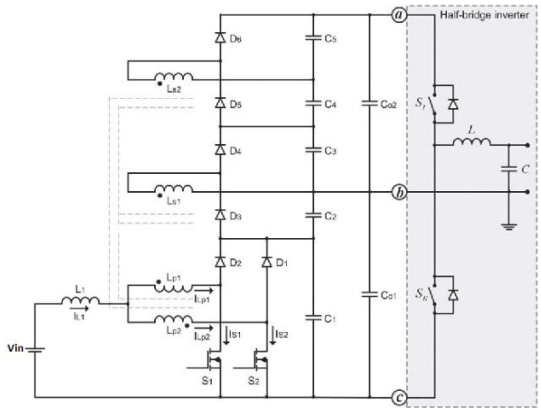

FIG 1: DC-DC boost converter using the 3SSC supplying a half-bridge inverter.

The topology in [18] corresponds to a lift converter using the 3SSC and one secondary coil, where the aforementioned advantages associated with the 3SSC are obtained [17]. additionally, for a given duty cycle, the static gain is often changed by properly adjusting the turns ratio without increasing the voltage stress for the active switches, which is a smaller amount than half the output voltage. during this structure, a part of the input power is directly transferred to the load without flowing through the active switches, thus implying reduced conduction losses. Unfortunately, this converter won't work properly when the duty cycle is less than 0.5 due to magnetic induction issues. In this context, this article presents the qualitative and quantitative analysis of a high-voltage-gain dc-dc boost converter, based on the 3SSC, which can be related, as shown in Fig. 1. In addition, the duty cycle can vary from D = 0 to D = 1 without affecting the regular operation of a converter, reducing the voltage stress for the diodes and increasing voltage gain by changing the turns ratio and some secondary windings. Other advantages of topology are studied in [18]. As guaranteed by the voltage around the converter, the output voltage remains balanced. The Neutral-Point Clamping (NPC) windings [19], a semiconductor and dual half-bridge inverters [20]. The first step is to show the operational phases of the converter. An experimental prototype is adequately implemented to validate the structure's theoretical behavior and discuss related issues.

II. PROPOSED DC-DC BOOST CONVERTER

The converter consists of V_{in} input voltage; the L_1 inductor; the T_r transformer attached to the active switch's S_1 and S_2; the D_1, D_2, D_3, D_4, D_5, and D_6 are rectifier diodes; the C_1, C_2, C_3, C_4, and C_5 auxiliary clamping's capacitors; and the C_{o1} and C_{o2} electrolytic capacitors. The operating phases of the boost converter are based on the current flowing through L_1. The converter will work with DCM, CCM, and CRM, all conditions are set by D>0.5 for Overlapping Mode (OM) or D<0.5 for non-Overlapping Mode (NOM), instead of the structure studied in [18], however, it is expected that qualitative analysis will be developed as follows for the CCM-OM. While the converter is suitable for CCM, the DCM mode or CRM.

Figure 2(a), 2(b), 2(c), 2(d) shows and describes the equivalent circuits representing the operation of a converter for one switching cycle. Fig. 3 shows the related theoretical waveforms.

2.1 First stage

$[t_0, t_1]$ [see Figure 2(a)]: S_2 is enabled, while S_1 is also enabled. In reverse biases are diodes D_1, D_4, and D_6, while also D_2, D_3, and D_5, respectively. In its respective magnetic field, energy is stored and the current flows through L_1, that is, IL_1 increases linearly. Part of these streams is passed by the recirculating L_{p1} and the rest of the L_{p2} and the S_2 switches because the existing distributions are retained. After all, the L_{p1} and L_{p2} recirculating systems are equally spaced. No energy transfer from the source of input into the charging system is provided by C_1, C_2, C_3, C_4, and C_5 auxiliary Capacitors. This stage finishes when the S_1 switch is turned off.

Operating stages for the proposed converter in CCM-OM is 2(a) First stage, 2(b) second stage, 2(c) Third stage, 2(d) Fourth stage

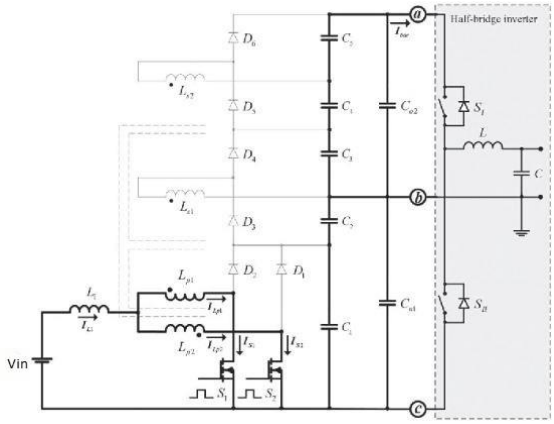

FIG 2(a): First Stage

The current through the inductor is observed from the below equation

$$L1 \cdot \frac{dI_{L1}}{dt} - V_{in} = 0 \quad (1)$$

The time interval that defines the stage is

$$t_1 - t_0 = \frac{T}{2} \cdot (2 \cdot D - 1) \quad (2)$$

2.2 Second Stage

(t_1, t_2) [Fig. 2(b)]: [t_1, t_2]: Switch S_1 is disabled at t=t_1 and S_2 is still activated. The magnetic flow is kept constant by the voltage around the inductor. S_1 and C_2 are identical in voltages. Diodes D_2, D_3, and D_5 are forward biased, but the diodes D_1, D_4, and D_6 have remained reverse biased. Current IL_1 is flowing linearly through the Primary windings L_{p1} and L_{p2}. The L_1 and also the source transmission energy to the C_1, C_2, and C_4 auxiliary capacitors, as well as to C_{o1} and C_{o2} output filter capacitors.

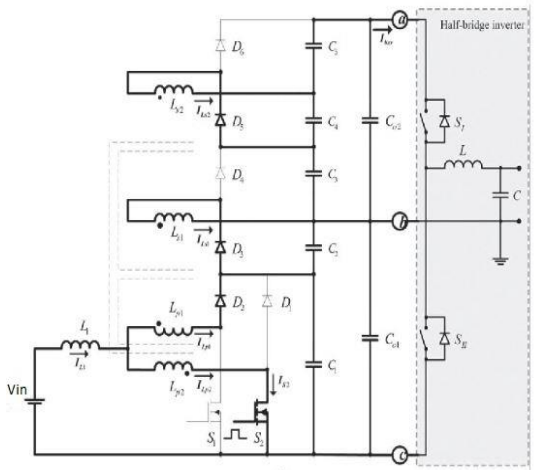

FIG2(b): Second Stage

The equation for this stage represents is

$$-L_1 \frac{di_{L1}}{dt} + \frac{V_{in}}{2(1-D)} - V_{in} = 0 \quad (3)$$

The correspondent time interval is

$$t_1 - t_2 = T_s \cdot (1 - D) \quad (4)$$

2.3 Third stage

[t_2, t_3] [Fig. 2(c)]: Switch S_1 is enabled at t = t_2, while S_2 is not enabled. The reverse bias of diodes D_2, D_3, and D_5 and the D_1, D_4, and D_6 diodes. Similar to the first level, there is no energy transfer into the load. In addition, the load is supplied by the auxiliary Capacitors C_1, C_2, C_3, C_4, C_5, and the output filter Capacitors C_{o1} and C_{o2}. This step ends when the S_2 switch is finally disabled. This stage is described by the differential equation as (1). The appropriate time interval is also defined (2).

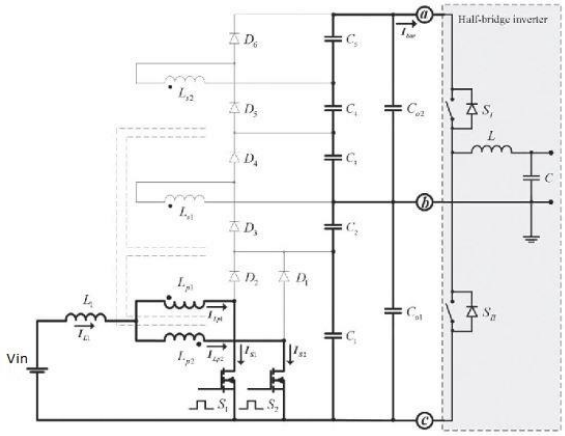

FIG 2(c): Third Stage

2.4 Fourth Stage

[fig. 2(d)], [t_3, t_4]: Switch S_2 has been turned off at t=t_3, but the S_1 is still on. The voltage is reversed over the inductor to maintain continuity of the magnetic flux. The voltage over S_2 is the same as the C_1 Capacitor. Forward bias is in diodes D_1, D_4, and D_6 while in reverse bias is in D_2, D_3, and D_5. The power is being transferred to auxiliary C_1, C_3, and C_5 Capacitors and C_{o1} and C_{o2} Capacitors in the second phase analogously to L_1 and the source. This step defines the differential equation (3), whereas the time interval is given as corresponding (4).

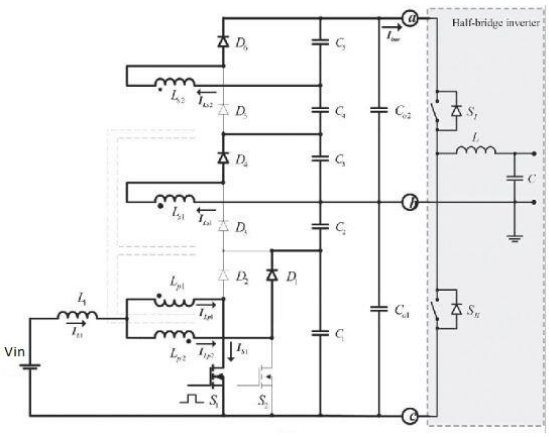

FIG 2(d): Fourth Stage

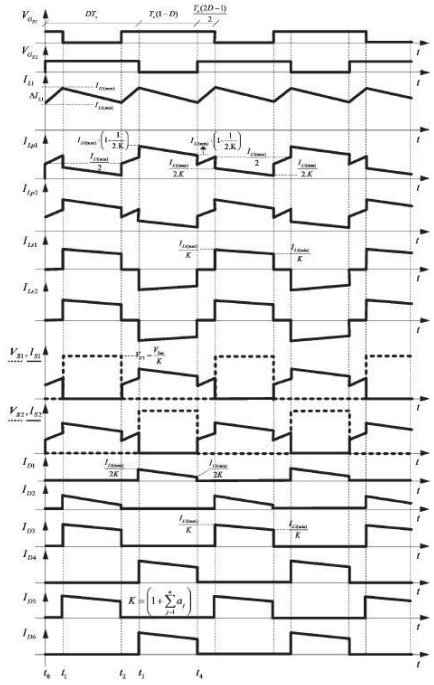

FIG 3: Theoretical waveforms for the proposed converter

B. Static Gain

The average voltage across the inductor $V_{L1(avg)}$ is null during the switching time T_s,

$$V_{L1(avg)} = 2 \cdot \frac{1}{T_s} \cdot \left[\int_{t0}^{t1} V_{in} \, . dt + \int_{t1}^{t2} (V_{in} - V_{LP}) \, dt \right] = 0 \quad (5)$$

Where V_{LP} is one of the highest voltages which is equal to L_{P1}, $L_{P2,}$ and V_{in} i.e., primary windings to the input voltage.

Substitute Equation (2) and (4) in (5) it will give

$$V_{in} \cdot \left[\frac{T_s}{2} \cdot (2 \cdot D - 1) \right] = V_{LP} . [T_s \cdot (1 - D)] - V_{in} [T_s \cdot (1 - D)] \quad (6)$$

The maximum voltage across the primary winding is

$$V_{LP(max)} = V_{LP1(max)} = V_{LP2(max)} = \frac{V_{in}}{2 \cdot (1 - D)} \quad (7)$$

The voltage across the capacitor C_1 is determined by Eq (8), The voltage across the generic capacitor is described by (9)

$$V_{C1(max)} = 2 \cdot V_{Lp(max)} \frac{V_{in}}{(1 - D)} \quad (8)$$

$$V_{C2.j\ (max)} = V_{C2.j+1\ (max)} = \frac{a_j \cdot V_{C1\ (max)}}{2} \quad (9)$$

The following ratio is also valid:

$$a_j = \frac{N_{Sj}}{N_P} \quad (10)$$

Where j is the number of secondary winding turns. Furthermore, the dimensionless quantity a_j is the ratio of the number of turns for a given secondary winding j. N_{Sj} is the no of turns for the primary winding Np. The output voltage V_{bus} will represent the sum of the voltage across the capacitor.

$$V_{bus} = \frac{V_{in}}{(1 - D)} \cdot (1 + 2 \cdot a) \quad (11)$$

Table-I

Parameter	Specification
Rated output Voltage	P_{bus}=1000 W
Rated load	Resistors R_{o1}=R_{o1}=320 Ω connected to capacitors
Minimum Input Voltage	$V_{in(min)}$=42 V
Maximum Input voltage	$V_{in(max)}$=54 V
Rated input voltage	V_{in}=48 V
Output Voltage	V_{bus}=400 V
Switching Frequency	f_s=25kHz
Ripple current through inductor L1	$\Delta I_{L1(max)} = 20\% I_{L1(avg)}$
Ripple voltage across auxiliary and output capacitors	$\Delta V_{C1.....C5} = \Delta V_{Co1} = \Delta V_{Co2} = 1\% \cdot V_o$
Expected theoretical efficiency	η=93%
Number of secondary windings	j=2
Turns ratio of the transformer	$a_1 = a_2 = a = 1$
Designed elements	
Inductor	L1=60 μ H
Main switches	MOSFET
Diodes D1..... D6	Ultrafast diode
Capacitor C1....C5	C1=202 μ F, Polyester, 400 V
Output capacitors Co1 and Co2	Co1=Co2=470 μ F, electrolytic, 450 V

$$V_{bus} = \frac{V_{in}}{(1-D)} \cdot \left(1 + \sum_{j=1}^{n} a_j\right) \qquad (12)$$

Finally, the static gain equation is described from the above equation

$$G_V = \frac{V_{bus}}{V_{in}} = \frac{1}{1-D} \cdot \left(1 + \sum_{j=1}^{n} a_j\right) \qquad (13)$$

III. SIMULATION AND EXPERIMENTAL RESULTS

The experimental prototype whose results are set out in Table I has, according to the procedure established in session II, been planned and implemented. Some waveforms are obtained and discussed below.

Consider the need for a dc bus rated 300 or 440 V used to supply DC-AC. In this case, of course, poor efficiency is obtained, as demonstrated in [17], if the classic boost converter is used. The basic boost converter is considered to be the base, which is also mentioned in [17] if it is specified that the non-isolated topology is sufficient for high voltage applications. This is the key explanation for the choice of the same point of operation as [17], Although the gain can be increased further, the gain is selected. There is also a presence and analysis of certain experimental waveforms.

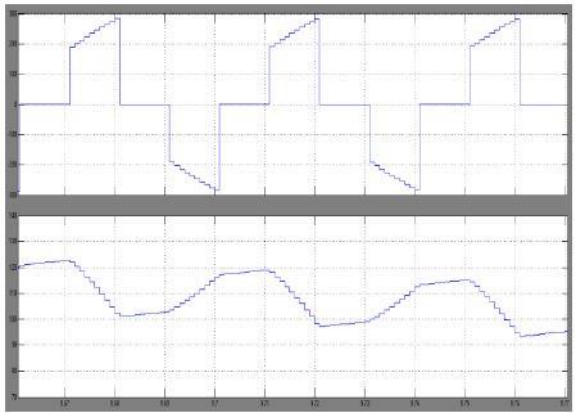

Fig. 4. Voltage and current waveforms in the primary winding Lp1 (VLp1 – 50 V/div., ILp1 – 20 A/div., time – 10 μs/div.)

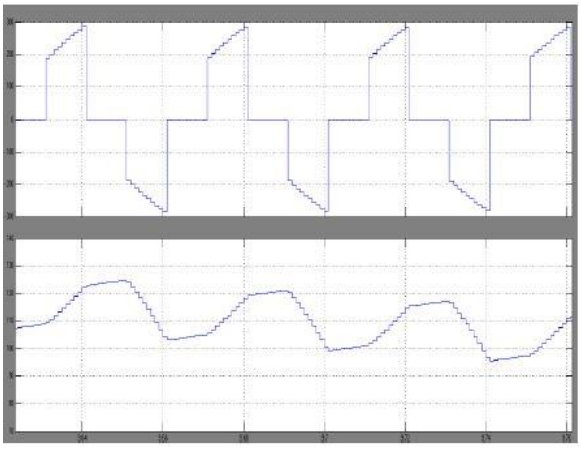

Fig. 5. Voltage and current waveforms in the primary winding Lp2 (VLp2 – 50 V/div., ILp1 – 20 A/div., time – 10 μs/div.)

The waveforms on the primary side of the transformer are shown in figures 4 and 5. There is good current sharing between the windings with reduced ripple.

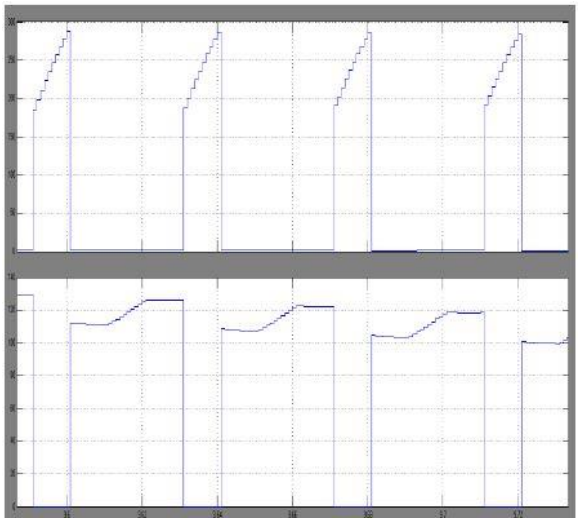

Fig. 6. Voltage and current waveforms for main switch S1 (VS1 – 50 V/div., IS1 – 20 A/div., time – 10 μs/div.)

For the main switches, FIG. 6 displays the waveforms. The voltage through switch S_1 is below half the power voltage so that reduced ON-resistance is possible with the use of MOSFETs. The waveforms for the diodes used in the converter are the corresponding figures 6 and 7. The maximum ratings for each of these are the values forecast in the theoretical analysis and the waveforms given in Fig. 3.

The converter's efficiency is less than with similar systems, e.g. [3] and [17]. The transformer in [3] is a high voltage gain and higher performance pull isolated topology. The static gain in this instance only depends on the transformer turning relation and the duty cycle, and the high efficiency of the rectifier diodes is due to an active clamp circuit with two active additional switches. Compared to the topology presented in this paper, the high complexity of the drive system and higher costs are predicted. In various applications, the work proposed in [17] uses VMCs comprised of diodes and Capacitors for increasing the static gain because non-isolated converters are preferred to isolated topologies. It is also shown that the number of cells and the duty cycle rely on certain parameters. Although the fig. 7. Diodes D4 and D6 waveforms (VD4, VD6 = 50 V/div, time = 10 μs/div).

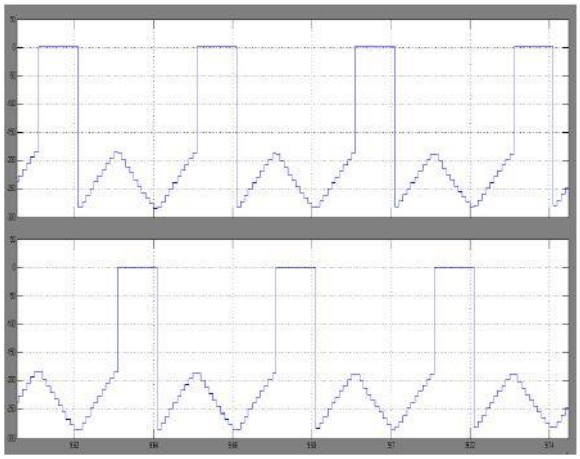

Fig. 7. Voltage waveforms for diodes D1 and D2 (VD1, VD2 – 50 V/div., time – 10 μs/div.)

This paper does not use VMCs and the static gain depends on the duty cycle, the number of secondary windings, and the ratio of turns between the main and the secondary sides. As the turning ratio and the number of secondary windings increase, the voltage tension across the main switches can be decreased. The voltage stress in the diodes, therefore, increases proportionately with the additional parameter, leading to increased losses in passive semiconductors. Trade-offs shall then take account of the performance, static gain, and count of components that have not been studied in-depth in this paper. The key contribution, on the other hand, is the proposed high-voltage converter dc-dc that is capable of supplying half-bridge and NPC inverters. The proposed converter is not so competitive with the chosen operating point that those in [3] and [17] are needed only to achieve a high voltage gain. It should otherwise be considered that the division dc-link inverters can be implemented equally.

CONCLUSION

This article has addressed a dc-dc power converter based on the 3SSC, which is suitable for supplying split capacitor inverters. Furthermore, the proposed topology is suitable for different applications, such as engine drives, PLC, or renewables. The converter's quantitative and qualitative analyses have enabled the proper design process to be used and tested for an experimental prototype. The conduct of semiconductor elements, waveforms, efficiency, and many other aspects is close to that predicted in

principle with regards to the static gain curves, current, and voltage stress.

From experimental waveforms, the converter is sufficient to supply half-bridge, dual half-bridge, and NPC inverters. The tension stress on the active switches is also reduced, enabling the usage and consequently high performance of lower-cost switches. The prototype has low size and volume because magnetics is designed to double the frequency of switching. In the entire load region, i.e., higher than 92 percent, good performance results even. It has also been demonstrated that the voltage balance of the output voltage Capacitors is maintained satisfactorily despite the unbalanced loads that are supplied due to 3SSC use. The main contribution is the proposed high-voltage dc-dc converter that provides semi-bridge and NPC inverters, however. In comparison with the selected operating point, the proposed converter is not so competitive that [3] and [17] are only necessary for high voltage gains. The division dc-link inverters should, otherwise, be considered equally applicable.

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