Toward Electronic Voting System: An Engineering Solution for Integrity and Trust of Record of Voting Systems

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Abstract- A major challenge in the proliferation of embedded microcomputer system is the design of the interfacing. The interfacing involves matching of signals, timing and provision of communication protocols between the microprocessor and the external devices. The paper presents the design and construction of a high speed electronic voting system using Intel microcroprocessor as an embedded microprocessor for a range of contestants. An EEPROM is used for storage with recoding capacity of 99,999,999 votes for each contestant per polling unit. The features include instant feedback on results of the polling unit, corrective procedure in its vote recoding and an estimated minimum rate of one vote per second. The system has a maximum power consumption of 3.75W and may be powered by mains, solar or battery for application in remote areas. The work presented aimed at engineering solution for integrity and trust of record of voting system.

Indexed Terms- Embedded systems, electronic voting system, buss contention, Initialization, Solar energy, Address decording, Microcontroller

I. INTRODUCTION

The microprocessor solution is becoming increasingly attractive for engineering problems that include information storage and retrieval, processing, control, monitoring and display. Programming microprocessor based system gives a great superiority because it can be made intelligent. It provides integrity of function and accommodates the control of the system. The role of microprocessors is immense. Almost all forms of consumers, industrial and military equipments use microprocessors and the challenge for application is increasing. However, design of communication interface between the microprocessor and external devices, matching of signals and timing requirements remains a challenge for every application.

II. ELECTRONIC VOTING MACHINES

Voting is decision making in democratic governance and a voting machine may be used to register votes. Election of candidates into public offices has been a contention in most developing nations because of various factors including lack of confidence in the voting system. Voting system in such countries has failed to translate the intent of the people into properly counted votes for decision making. This then present the design, construction and analyses of an embedded microprocessor based voting machine that is efficient and provides desired integrity of the registered votes.

Electronic voting system has been in use since the 1960s when punch card system debuted. Internet and telephone voting system have gained popularity for non-governmental purposes since the 1980s but suffer security problems which prevent their application for government election.

2.1 Basic Requirements of Electronic Voting Systems

1. Accuracy: the goal of any voting system is to establish the intent of each individual voter and translate those intents into final tally. To the extent that voting system fails to do this it is undesirable. Accuracy is how well the entire process translates the voters' intents into properly counted votes. This characteristic includes security i.e. it should be impossible to change some one else vote or otherwise affect the accuracy of the final tally.
2. Anonymity: Secrete ballot are fundamental to democracy and voting system most be design to facilitate voters' anonymity.
3. Scalability: Voting system should be able to handle large elections. The complexity of election is

another issue unlike many countries where the national election is a single vote per person or a party, a Nigerian voter is face with dozens of individual election e.g. national, local government election and everything in between.

4. Speed: voting system should produce result quickly. This is particularly important in countries where people expect to know the result of the day's election before bed time. It is less important in other countries where people don't mine waiting for days or even weeks before the winner is announced.

2.2 Problem resulting from manually counted paper ballot system

The voting method used in many developing countries e.g. Nigeria is associated with the following short coming:-

1. Human error: since the votes are manual counted, it is subject to human error.
2. Misrepresentation: After counting the votes, a different result is often recorded and announced. The people counting the votes often misrepresent the vote of their preferred candidate over the other opponents.
3. Poor time management: its takes long time to finish counting the votes of the various polling units before the final result is announce.
4. No corrective measure: when some one thumbprint in the wrong location or in an undefined place (border) the vote is lost.
5. Voters have no idea of the votes of the various contestants during and at the end of the election right there at the polling unit, that is why any figure can be announced latter.
6. Omission of some parties in the ballot paper.

2.3 Operation of the designed voting system

The microprocessor based voting system presented in this paper is designed for various elections with each election result stored in separate. Voters will be giving passcard after registration in form of scratch cards. The system will pulled the key of each voter during the election exercise, if valid, it will be accepted, and if the same key is used again for the same election, an error message will be display indicating that the key has been used or is invalid, hence preventing multiple votes. A sensor located at the entrance of the polling unit increases the security of the system. When an entrance is acknowledged, the busy LED will be on and no password will be accepted until the person inside comes out. When the voter press the key assign to the candidate of his choice, the initials of the party will be displayed for him to verify if that is his actual intent, if yes, the same key can be pressed again or else another choice of key is pressed. Once the key is press the second time, the candidate has no any other chance, the votes of that contestant plus the present one will be displayed, thus providing a progressive instant feedback results. As the voter goes out, the display will blank to ensure that his intent is kept secret thereby facilitating voters' anonymity. Once a vote is acknowledge, even if the person keep on pressing the same key or other keys it will not be accepted i.e. only one vote per person. The result of the entire election will be known at the polling unit and can be uploaded to a central server. No body can be able to vote without a valid voter card. From the number of registered cards, the expected maximum possible number of total votes to be casted in each polling unit will be known before the election.

III. MICROCONTROLLER DESIGN

Each peripheral or memory location is identified with a unique binary number called an address. The microcontroller is designed using partial address decoding using INTEl 8085 microprocessor along with the following periferals: 27C512 EPROM, 8255 programmable input/output port, 8155 RAM/port, 8279 keyboard and display controller, and 28C64 EEPROM [2][5]. The chip select equation of the periferals are as shown in equations 1 to 5 while the external and internal address decoding for each chip is shown in table 1,

Chip select equations:

$CS_0 = A_{15} + A_{14} + A_{13}$, 27C512 (EPROM) (1)

$CS_1 = A_{15} + \overline{A}_{14} + A_{13}$, 8255 (Port) (2)

$CS_2 = A_{15} + \overline{A}_{14} + \overline{A}_{13}$, 8279 (Keyboard encoder/display driver) (3)

$CS_3 = \overline{A}_{15} + A_{14} + A_{13}$, 8155 (Port/RAM) (4)

$CS_4 = \overline{A}_{15} + \overline{A}_{14} + A_{13}$, 28C64 (EEPROM) (5)

Table 1: Address Decoding

CHIP	CAPACITY	USED CAPACITY	STARTING/ END ADDRESS	ESTERNAL DECODING ADDRESS A_{15} A_{14} A_{13}	INTERNAL DECODING ADDRESS
EPROM 27C512	64KB	4KB	0000-0FFF	0 0 0	A_0-A_{11}
Port 8255	4bytes	4bytes	4000-4003	0 1 0	A_0-A_1
Keyboard encoder 8279	3bytes	3bytes	6000-6100	0 1 1	A_8
Port/RAM 8155	256bytes	256bytes	8000-80FF	1 0 0	A_0-A_7
EEPROM 28C64	8KB	8KB	C000-DFFF	1 1 0	A_0-A_{12}

3.1 System Bus Design

A bus is a communication path consisting of parallel wires (Conductors) designed to transfer information between modules or cards in a microprocessor system. It is an electrical highway linking the microprocessor and the peripherals. The system bus consist of three subbuses namely: The data bus, address bus and the control bus [1][2][3][4][5].

3.1.1 Factors influencing bus design

There are three factors influencing the design of a bus, these are:

1. mechanical specification
2. electrical specification
3. protocol

The mechanical specification governs the physical aspect of the bus (that is size, material and connectors), the electrical specification governs the requirement that must be met by the signals on the bus while the Protocol governs the sequence of signals that must be complied with to secure an orderly exchange of data.

3.1.2 Mechanical Specification of a Bus

In this research work, the contact between the system bus and the memories or peripherals is established via IC based with each components positioned as closed as possible to the system bus. The space between the pins meets up with the standard for bus which is about 0.1 to 0.15 in pitch. This type of bus mechanics is highly reliable since it is not subject to wear and tear due to repeated memory card insertion and removal or to corrosive agents which can lead to intermittent contact between the chips and the system bus. Though this type of contact can be affected by gradual increase of dirt, any faulty chip can easily be change without desoldering the components.

3.1.3 Electrical Specification of a Bus

There are certain electrical realities that must be considered in bus design. The electrical realities that are vital to the electrical characteristics of bus design are: Bus driver, bus contention, bus transmission properties and bus arbitration [1].

- Bus drivers

Although digital systems operates with logical 0 and logical 1 level, when considering the interconnection of logical elements to the system bus, two sets of characteristics must be satisfied, that is, those relating to the voltage levels and those relating to the current levels. In certain application depending on the number and types of chips used in designing the microcomputer, the processor may not be able to meet up with these two requirements. . In this research, a transparent latch (74373) is used which served a dual function of demultiplexing the data bus from the address bus and as address bus driver.

- Bus Contention

This is a situation where two or more chips (modules, memory or I/O device) or buffers attempts to drive the data bus simultaneously. Another term for bus contention is bus conflict. Both dynamic and static buss contensions were mitigated by using 74138 active low output decoder for external decording or selection of the chips. For processor with the same pin for both read and write control signals, the two signal should be separated via not gate and be used in enabling the decoder to mitigate dynamic bus contention as shown in Fig 1(a). The processor used in the research has distinct pins for read and write control signals, hence the connection is as shown in Fig 1 (b).

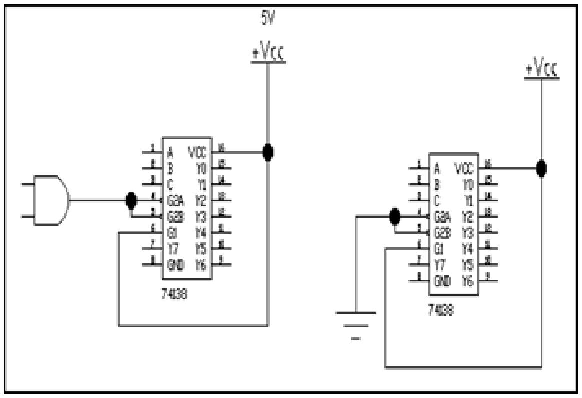

Fig.1: Decoder connection

- Bus Transmission Characteristics

System bus consists of parallel wires having properties similar to transmission line. A sharp switch signal at the transmission end is often received as a slowly charging signal at the far end of the cable. Considering Fig 2 (c) when a step voltage V is applied in the line, this step voltage corresponds to the transition from zero to one in a digital system. Because of the electrical properties of matter, it is not possible for the signal to travel down the circuit instantaneously. The resistance, inductance and capacitive effect of the bus affect the way the pulse flow down the circuit. The propagation delay of the pulse on the bus is √LC second per unit length, where L is the inductance and C is the capacitance of the bus both in per unit length. There are two transmission line effects that should be considered when designing a system bus, these are propagation delay which is related to the voltage effect and multiple reflection which is the bus current effect. If the ratio of the rise time to propagation delay is less than 0.5, the bus system should be treated as a transmission line [1]. In other to avoid the negative effect of propagation delay, the maximum path length of the system bus designed in this research is 16cm (0.16m).

For multiple reflections of the signal at the end, considering the three limiting cases:

1. Match line: The load impeadance is equal to the bus characteristics impedance, no reflection, equation (6)

$$V_r = V_i \frac{R_T - R_T}{R_T + R_T} = 0$$

$$R_T = Z_o \qquad (6)$$

2. Short circuit line: Inverted pulse reflected, equation (7)

$$V_r = V_i \frac{0 - Z_o}{0 + Z_o} = -V_i$$

$$R_T = 0 \qquad (7)$$

3. Open circuit line: Pulse reflected, equation (8).

$$V_r = V_i \frac{\infty - Z_o}{\infty + Z_o} = V_i$$

$$R_T = \infty \qquad (8)$$

Where:
Z_o = Characteristics impedance, $Z_o = \sqrt{L/C}$
R_T = load impedance
V_T = Voltage across the terminator
V_i= Incident voltage

In practice perfect matching is realy possible, but there are three things that can be done to minimize the effect of multiple reflection, these are:

1. Each signal should be given time for all reflections to die to a very small proportion. The content of the address and data bus should not be sampled until 100ns after they are normally valid. In his application, the operating frequency is 1.95MHz, the time for one T-state is 512.8ns, therefore, even if the bus should be sample in the next T-state, all reflected signal must have died away.
2. Another way of minimizing multiple reflections is to terminate the bus with 100Ω
3. Lastly, the bus should be loaded as little as possible and long stubs should be avoided if possible. A stub is an extension to the bus rather like a T-junction, [1].

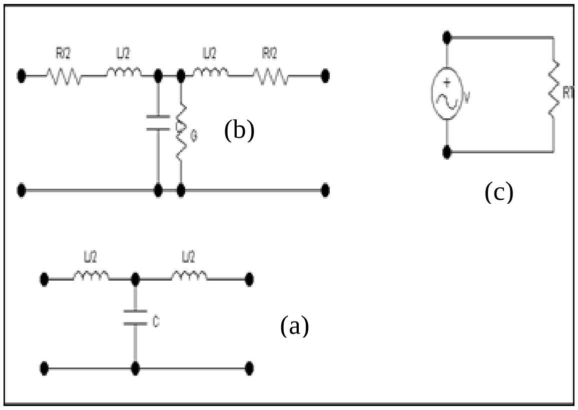

Fig.2: Bus transmission line

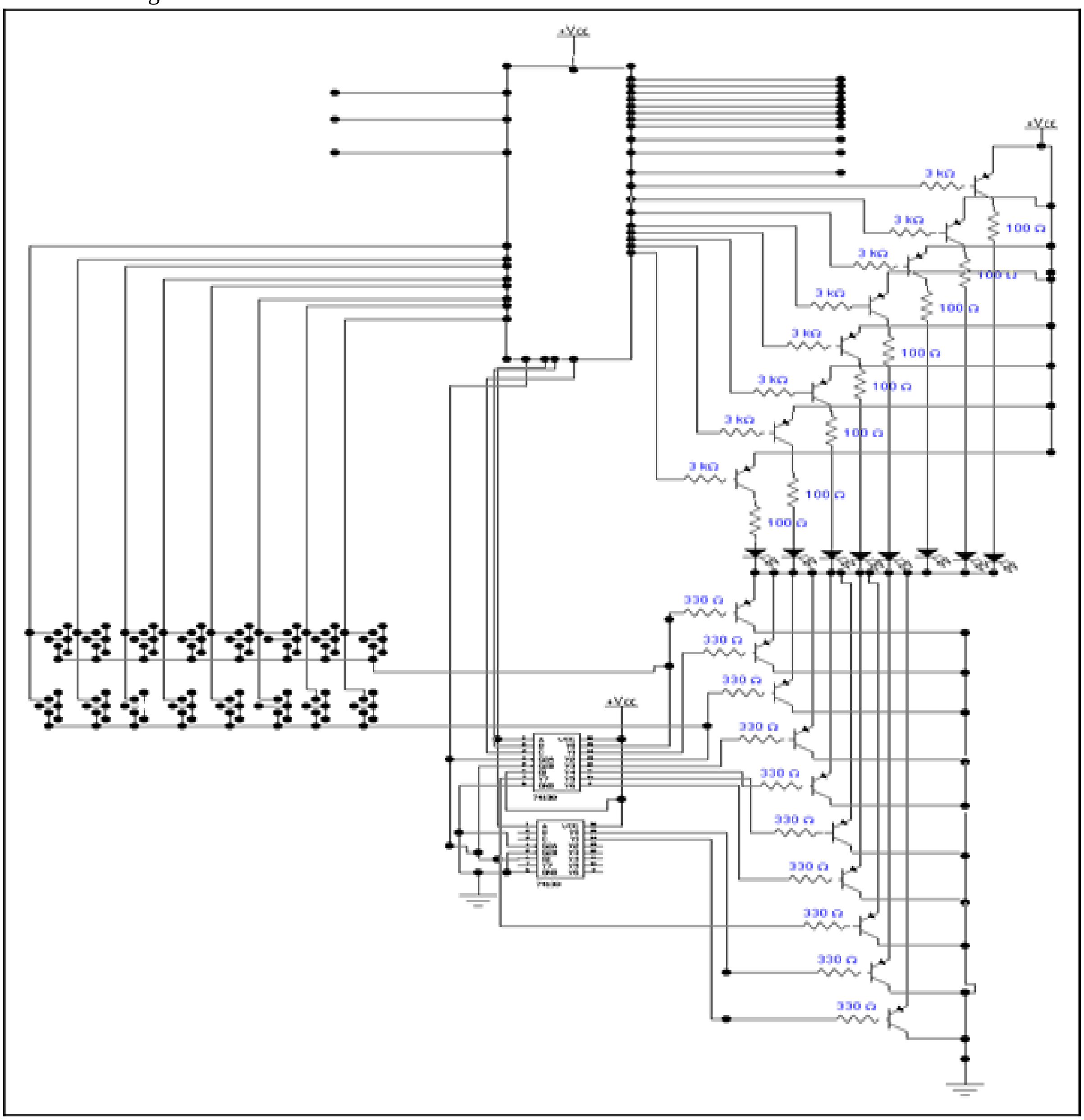

Fig.3: Keyboard and display encoder using INTEL 8279

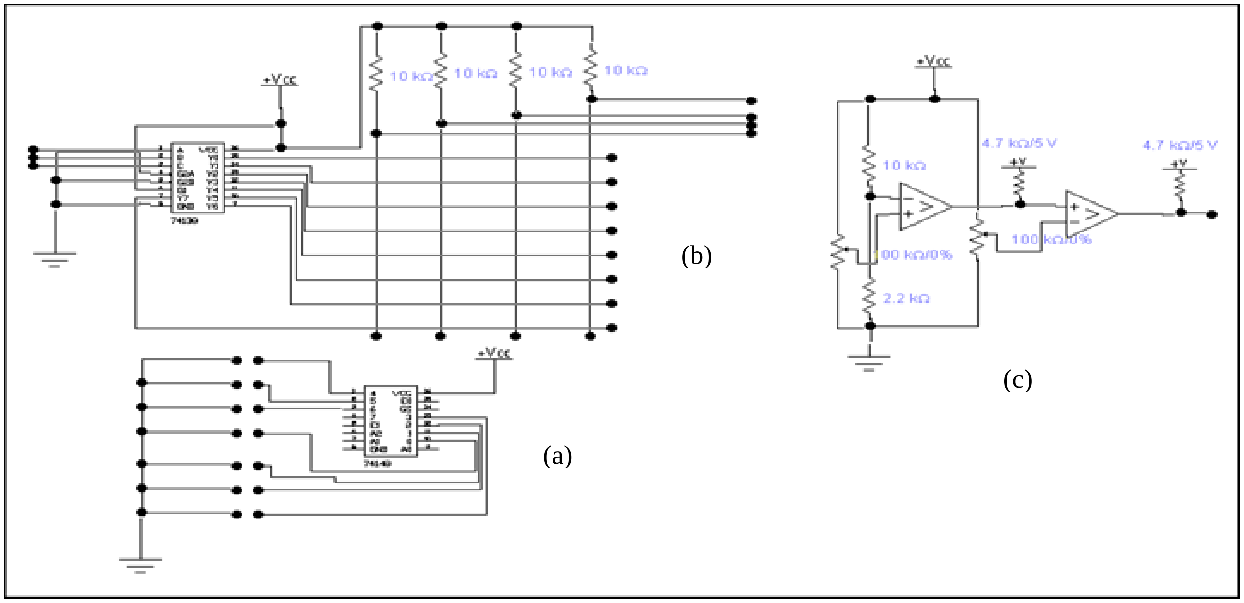

Fig.4: (a) Functions keys, (b) Parties keys and (c) sensor circuit

IV. TEST AND RESULTS

Microprocessor based systems hardly ever been completely built and tested as a complete system. A completely built system is difficult to troubleshoot. Traditional approaches such as signal injection and isolating trouble spots are not effective for troubleshooting bus oriented systems. Therefore, the system is built and tested in stages. Each subsystem e.g. the keyboard, display, sensor and memories are built and tested separately as independent modules using an in-circuit emulator

There are two major principles often used in testing bus oriented systems, these are:

1. Borrowing resources from a working system
2. Substitution approach

These principles are used in testing each separate subsystem of the microprocessor based system. A working system is needed that can create an environment similar to the complete prototype system and that is generous enough to share its resources with the hardware module to be built, such a working system is called an in-circuit emulator. Other instruments that can be used to test bus oriented systems where there is constant flow of data which continuously changes logic states are logic analyzer and signature analyzer [5]. None of the above mentioned instruments was available to test this research work rather a circuit was built and interface with an existing working general purpose microcomputer designed using 6802 microprocessor to serve as an in-circuit emulator [8]. Each section of the electronic voting system was tested one at a time using the in-circuit emulator until the entire system was finally coupled and tested. In this final stage, total software and hardware were integrated for testing. A hardware prototype can be viewed as a foetus growing in the womb of an in-circuit emulator until the fetus is fully developed and functioning independently, the in-circuit emulator provides the entire necessary environment and the resources. Must of the design time was spent on software debugging as compared with the time spent on hardware.

4.1 Power Supply: Solar panel response

The important of electrical power supply in any intelligent system can not be over emphasized. As stated, the system can be powered with either solar, battery or mains. The effect of solar intensity on the open circuit voltage, load voltage and current is depicted in table 2 and presented graphically in Fig 5. For any closed circuit voltage below 6.6V, the system fails to perform the expected function. This is because the switching between the sources of power supplies is carried out using solid state semiconductors (diodes) which causes a voltage drop of 0.6V before the input of the 5V regulators which need at least 6V at there inputs in other to function satisfactorily.

When the input voltage is at least 6.6V, the current remains fairly constant between 0.36A and 0.37A up to the rated voltage of the panel. A well designed regulator need only small bias current within the rated input voltage range. Hence this current is the actual current sink by the system at constant 5V. Even if the no load voltage of the panel is high, and the solar intensity is low, on loading the system, the voltage drop to such a small value resulting into small current which is insufficient to drive the system.

4.2 Battery Response

The system was powered with 12V, 100AH for eighteen hours within two consecutive days. The first day, it was powered for six hours from 2:36 PM to 10:36 PM at an initial terminal potential difference of 11.77V and run down to 10.50V, Fig 6. The current drawn by the microcontroller is 0.365A at constant 5V. The next day the system was tested for twelve hours continuously from 7:25 AM to 7:30 PM. After twelve hours the terminal potential difference dropped to 7.30V, Fig 7. When 1.8w fan was connected to the system, the current drawn increases to 0.538A. Based on this current, if the system is powered with fully charged 12V, 100Ampere Hour, the time taken before the battery will completely run is:

Time = $\frac{100}{0.538} = 185.874$ hours. Therefore, it can be powered with 12V, 100 Ampere Hour battery for one week seventeen hours without failure.

CONCLUSION

A fully functional microprocessor based electronic voting system that meets up with the requirements of a voting system was realized. The power consumption is 3.75w and can be powered by solar, battery or mains for remote application. The switching from one power source to another is automatically achieved using solid state semiconductor devices.

Table 2: Solar panel response

No load voltage (V)	Full load Voltage (V)	Current (A)	System response
12.36	3.99	0.01	Fail
17.89	4.49	0.19	Fail
17.93	4.51	0.19	Fail
17.72	4.39	0.12	Fail
17.78	4.48	0.26	Fail
18.63	5.00	0.32	Fail
18.68	5.46	0.34	Fail
18.60	6.74	0.35	Function
18.83	6.67	0.35	Function
18.39	6.88	0.36	Function
18.80	6.89	0.37	Function
18.55	7.12	0.35	Function
18.72	7.22	0.36	Function
19.06	7.09	0.37	Function
18.35	7.11	0.36	Function
18.75	8.30	0.36	Function
18.37	9.20	0.36	Function
18.81	12.40	0.36	Function
19.18	13.39	0.37	Function
19.05	14.60	0.37	Function
19.11	14.80	0.36	Function
18.81	14.86	0.36	Function
18.75	15.26	0.36	Function
18.58	16.93	0.36	Function
18.47	17.70	0.37	Function
18.70	17.80	0.37	Function
19.40	17.99	0.37	Function
19.03	18.22	0.37	Function

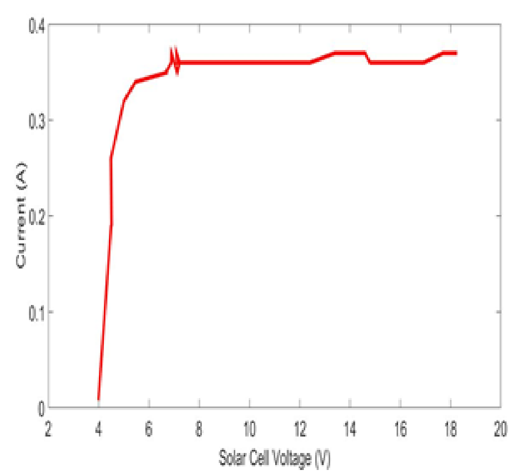

Fig. 5: Solar cell current against voltage

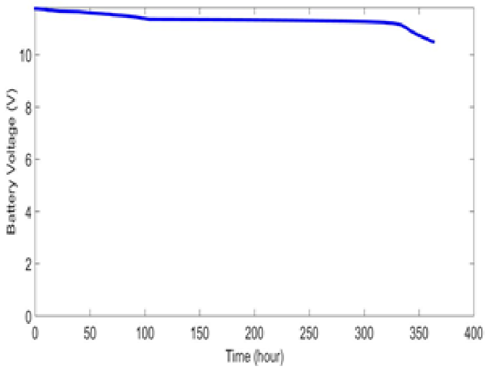

Fig. 6: Battery voltage for six hours

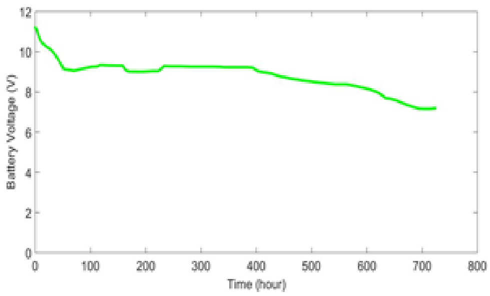

Fig. 7: Battery voltage for twelve hours

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