Modern Circuit Integration Techniques: Integrated Circuit Processing Sequence of Wafers Obtained from Czochralski Crsytal Growth Process

OYUBU, A.O[1], ONYEORU, H.C[2], ILOH, J.P[3]
[1, 2]*Department of Electrical/Electronic Engineering, Delta State University, Abraka, Oleh, Campus, Nigeria*
[3]*Department of Electrical/Electronic Engineering, Chukwuemeka Odumegwu Ojukwu University, Uli, Nigeria*

Abstract- ***The Czochralski process, a technique of growing crystal that is employed to get single crystals of semiconductors, metals, salts, and gemstone, is employed in growing high-purity semiconductor grade silicon ingot that are sliced into wafer-the fundamental material for integrated circuit (IC) fabrication. The wafers obtained from silicon ingots grown through the Czochralski process have: better resistance to thermic strain, better rate of fabrication, low cost of production, and immense oxygen concentration that provides the chances of internal gettering. This paper outlines the chain of the different processing steps involved in integrating wafers gotten from silicon crystal obtained from the Czochralski growth process.***

Keywords- ***Czochralski, Wafer, integrated circuit, silicon, crystal, Gettering***

I. INTRODUCTION

An integrated circuit, generally known to be an IC, is a minute arrangement of electronic circuitry and parts that are already infused or impressed on the exterior of a single crystal, or wafer of a semiconductor like silicon. It is so called an integrated circuit because the parts, circuitries, and substrate are pieced together, or constructed from a sole wafer of silicon, unlike in discrete circuitry in which the parts are crafted individually from separate materials and coupled thereafter. ICs rank in sophistication from very simple logic modules and amplifiers to complete microcomputers housing millions of building blocks.

The production of microscopic electronic circuitry and their use in computers and communication devices epitomized key invention of the twentieth century [1] [2]. These have culminated in the opening of novel concepts and applications that could not be implemented using discrete devices. Integrated circuitries on a sole silicon wafer which is increased to house more of such circuitries serve to considerably diminish the cost, while at the same time expanding the dependability of these circuitries.

Semiconductor devices are formed from semiconductors such as germanium, silicon and compound semiconductors like gallium arsenide, GaAs. Of all the known semiconductors, silicon has some distinct strengths which are absent in the others. A notable benefit of silicon coupled with its voluminous accessibility in nature in the form of sand and quartz is its formation of a high-grade stable oxide, SiO_2 which offers a high-quality insulating property. Silicon also remains the major semiconductor in the industry at present. The initial form of silicon that fabricators of devices and integrated circuitries utilize is a circular slice called wafer. These wafers' sizes range from 10-20 cm with a maximum of about 30 cm. Silicon must be in crystalline form, very pure, without defects, and also uncontaminated for it to be used.

Modern circuit integration techniques require very many steps, each of which comprises a sequence of basic operations. A number of these steps/operations are executed repeatedly during the course of the manufacture. The Czochralski process, the technique for obtaining high-purity semiconductor standard

silicon ingots that are sliced into wafer-the fundamental material for integrated circuit (IC) fabrication, will be discussed accompanied by an exhaustive view of the procedures associated with modern circuit integration techniques.

II. THE CZOCHRALSKI PROCESS

The Czochralski process is a technique employed in growing single crystal of semiconductor, metals, and a lot of oxide crystals [3]. The highest use may be in growing of very large cylindrical ingots or balls of single crystal silicon that is normally composed of quartz.

The melt is kept at a temperature of 1690K, which is a little higher than the melting point (1685K) of silicon. An accurately controlled amount of dopant impurity atoms like boron or phosphorous could be introduced to the molten intrinsic silicon so as to dope the silicon, thereby transforming it into N-type or P-type extrinsic silicon. This controls the electrical conductivity of the silicon. The proportion of the concentration of impurities in the solid, C_o ,to that in the liquid, C_t, is named, the equilibrium segregation coefficient k_o.

$$k_o = C_o/C_l \quad (1)$$

A seedcrystal, (a small highly perfect crystal), attached to a holder and possessing the desired crystal orientation is inserted in the molten silicon and a small portion is allowed to melt. The seed crystal's holder is drawn up and revolved as well. By accurately manipulating the temperature gradients, speed of pulling and speed of revolving, it is feasible to pull-outa sizeable single-crystal cylindrical mold from the melt. This technique is generally carried out in an inert sphere like argon, and in an inert compartment chamber like quartz

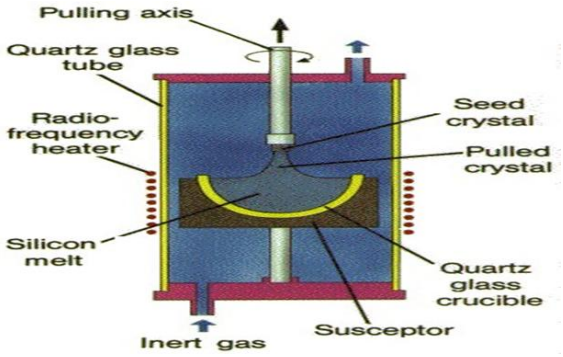


Figure 1: High purity semiconductor standard silicon being melted in a radio frequency heater [4].

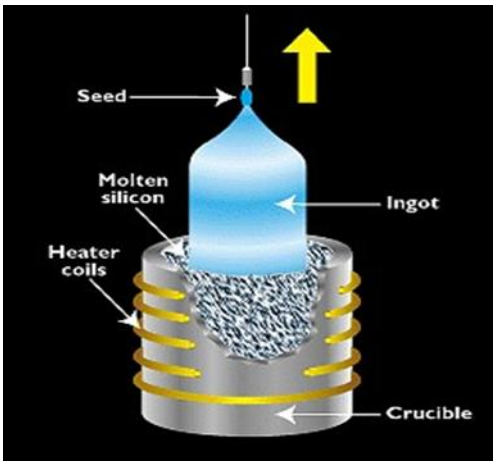


Figure 2: Single crystal ingot in a crucible [4].

2.1 Silicon Mold Cutting and Wafer Preparation

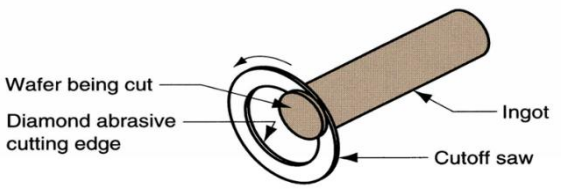


Figure 3: A single ingot being sliced into wafer utilizing a diamond abradant cut-off saw [5].

Finally, when the mass of the melt is already obtained, the crystal size is reduced. The reduction is done until there is a point of contact with the melt. The ingot that results from this process is cooled, removed, and sliced into wafers. The diameters of the ingots are around 200mm; recent ingots are about 300mm in diameter with length of 100 cm.

Slicing the wafers that are employed in the manufacture of integrated circuits is a process that involves accurate tools. The objective is to create

slices that are thoroughly flat, uniform, and without injury to the crystal frame.

The wafers are put through many steps which include lapping, polishing and chemical etching. Thereafter, the wafer sliced are cleansed, rinsed and dried to be utilized in the making of discrete systems and integrated circuitry

Figure 4: Sliced wafers[4].

III. THE BASICS PROCESSING INTEGRATED CIRCUIT

Every semiconductor integrated-circuit manufacturng process begins with a filmy piece of silicon,also known as substrate or wafer as depicted in Figure 4. The substrate is sliced from a single crystal of grown bar and polished to its final dimension with atomic smoothness.Most circuit designs dovetal in a few square centimeters of silicon area. Each partition is called a die. After production,the wafer is cut to form independent rectangular dies otherwise called chips.The chips are packaged to produce the final components .

A specific sequence or process of chemical and mechanical modifications is performed on certain parts of the wafer. Although complex processes employ an array of techniques, a basic IC processing will employ one of the following three modifications to the wafer:

- Implantation: Atoms or molecules are inputed to the silicon wafer, thus changing its electronic properties.
- Deposition: Substances such as metals, insulators, or semiconductors are inputted in filmy layers (like painting) onto the wafer.
- Etching: Substances are removed from the wafer through chemical reactions or mechanical motion.

IV. PHOTOLITHOGRAPHY

In each of the steps involved in the processing, a region on the chip is covered utilizing a suitable optical mask to enable desirable processing steps to be carried out on the remaining parts. The various processing steps include a wide range of tasks such as oxidation, etching, metal and polysilicon deposition, including ion implantation. The method used in accomplishing this distinctive masking, known as photolithography, is employed all through the course of the manufacturing. Figure 5 is a depictive outline of the various procedures involved in a normal photolithographic process.

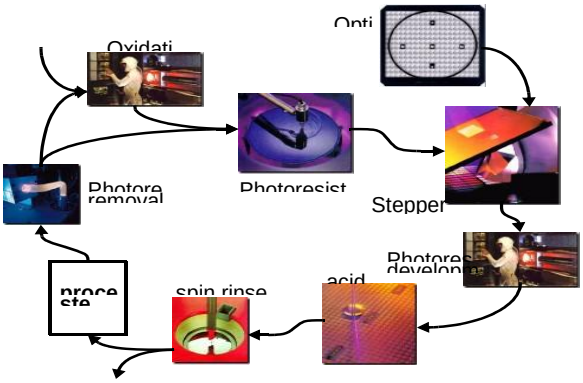


Figure 5: Typical operation in a single photographic cycle [6]

The following activities can be noted:

a) Oxidation surfacing — this step though optional, involves depositing a thin layer of SiO_2 over the entire wafer by airing it to a mix of high-purity oxygen and hydrogen at ± 1000°C. The oxide is applied as an insulation layer and forms transistor gates too.

b) Photoresist covering — a photosensitive polymer (akin to latex) is uniformly smeared while rotating the wafer to a girth of about 1 µm. This material by origin is dissoluble in an organic solvent but possess the potentials that the polymers crosslink when opened to light, rendering the affected parts indissoluble. This kind of photoresist is also known as negative photoresist. A photoresist which possesses the opposite qualities, i.e , which by origin is indissoluble but dissoluble after it has been exposed is a positive photoresist. Employing both positive and negative resists, a single mask may be utilized for two stages, making complimenting

sections ready for processing. Because the budget of making mask increases with advancement in technology, a decrease in the quantity of masks is very important.

c) Stepper exposure — a mask made of glass (or reticle), having the desired pattern to be transferred to the silicon is brought in contact with the wafer. The mask is non-transparent in the sections that are to be worked on and translucent in the other sections (assuming a photoresist that is negative).The glass mask may be seen as the negative of one layer of the microcircuit. The mix of both mask and wafer is now opened to ultra-violet light. The portion where the mask is translucent, the photoresist becomes indissoluble.

d) Photoresist development and bake — the wafers are developed either in an acid or base liquid so as to remove those areas of the photoresist that were not exposed. The moment the exposed photoresist has been removed, the wafer is soft-baked at a low temperature to harden the rest of the photoresist.

e) Acid Etching — this is done to selectively clear material from the areas of the wafer that are not masked by the photoresist. This is realized using different kinds of acid, base, and caustic liquids based on the materials to be removed. Much of the work with chemicals takes place at large wet benches where distinct solutions are made for particular process. Due to the hazardous attribute of some of these cleansing agents, safety and impact on the environment must be of primary concern.

f) Spin, rinse, and dry — here, a specialized tool (called SRD) cleanses the wafer employing deionized water after which it dries it with nitrogen. The micro-diameter size of current semiconductor systems implies that even the minutest particle of dust or dirt may damage the circuit. To forestall this from taking place, the various steps involved in the processing are performed in an ultra-clean environment in which the quantity of dust particles per cubic foot of air is between 1 and10. Automatic wafer handling and robotics are employed as much as possible. This is why the budget for a state-of-the-art fabrication facility is in several billions of dollars. Outside this, the wafer must be cleaned always to prevent contamination, and to eliminate the remnant of the preceding processing steps. Various process steps — the unmasked area is now put through an array of processing steps, namely; ion implantation, plasma etching, or metal deposition.

g) Photoresist removal (or ashing) — here, a highly heated plasma is employed in carefully removing the remaining photoresist without destroying the device's layers.

V. IMPLANTATION

There exist two approaches for introducing dopants—diffusion, and ion implantation. In both methods, the region to be doped is unmasked, as the rest of the wafer is smeared with a layer of buffer material, typically SiO_2.The two methods are discussed below:

a) DIFFUSION

This is carried out in a furnace while a flow of gas is running over the wafers (Just like in oxidation, except that a different gas other than oxygen is used). Many steps of the integrated circuit manufacturing process require a change in the dopant's concentration of some parts of the material. The formation of the source and drain regions, well and substrate contacts, the doping of the polysilicon, and the alterations of the device limits are examples of such.

In diffusion implantation, the wafers are placed in a quartz tube enclosed in a hot furnace. A gas carrying the dopant is sent into the tube. The very high temperatures of the furnace, typically 900 to 1100 °C, cause the dopants to be infused in the exposed surface both vertically and horizontally. The final dopant's concentration is the greatest at the surface and decreases in a Gaussian profile deeper in the material.

b) ION IMPLANTATION

In ion implantation, dopants are introduced as ions into the material. The ion implantation device controls and moves a stream of refined ion across the semiconductor surface. The speed of the ions predicates the extent they will enter the material, whilst the beam current and the duration of exposure

predicates the dose. The ion implantation technique gives room for an independent control of depth and dosage. This is why ion implantation is characterised by largely displaced diffusion in modern semiconductor manufacturing.

Ion implantation has some unfortunate side effects however, with the most prominent one being lattice damage. Nuclear collisions during the high energy implantation cause the displacement of substrate atoms, leading to material defects. This side effect is generally solved by employing an annealing procedure wherein the wafer is superheated to about 1000°C for 15 to 30 minutes, and left to slowly cool down. The heating process causes thermal vibration of the atoms which makes the bond to reform.

VI. DEPOSITION

Semiconductor manufacture procedure demands a repeated deposition of layer of material over the entire wafer to either provide buffering for a processing step or act as an insulating or conducting layers. Deposition may be achieved using many techniques especially the:

Chemical vapour deposition, CVD, where an appropriate reactant material is infused in a carrier gas that passes over the surface of the hot substrate. The heat emanating from the hot substrate surface prompts the reactants and the carrier gas to react chemically thereby forming the desired thin film on the surface of the substrate [7].

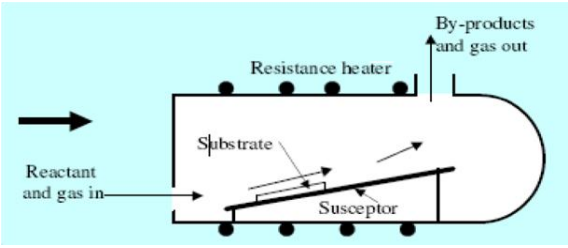


Figure 6: Chemical vapour deposition (CVD) system [8].

II. Physical vapour deposition, PVD, wherein a thin film of material is deposited on the surface of the substrate. In PVD, the material to be deposited is transformed into vapour by physical means and the vapour is conveyed over a zone of low pressure from source to the substrate. The vapour undergoes condensation on the surface of the substrate and becomes the thin film. Unlike CVD, which operates at elevated temperature, the PVD (physical vapour deposition) is performed at room temperature.

Different materials require different techniques which include: PVD sputtering, PVD by evaporation and Epitaxy which is about the same thing that occurs in CVD processes. For instance, silicon nitride (Si_3N_4) is utilized as a sacrificial buffer material during the formulation of the field oxide and the addition of the stopper implants. This silicon nitride is deposited everywhere employing a technique known as chemical vapour depositionor CVD, which uses a gas-phase reaction with energy supplied by heat at around 850°C.

Polysilicon, on the other hand, is deposited employing a chemical deposition process, which discharges silane gas upon the hot wafer coated with SiO_2 at a temperature of about 650°C. The resultant reaction yields a non-crystalline or an amorphous material known as polysilicon. To increase the material's conductivity, the deposition must be accompanied by an implantation procedure.

The Aluminium interconnecting surfaces are typically assembled employing a method known as sputtering. The aluminium is vaporized in a vacuum, with the heat for the vaporization conveyed by electron-beam or ion-beam bombarding. Other metallic inter-connect materials such as Copper require different deposition techniques.

VII. ETCHING

Etching is simply themethod of clearing materials like oxide or other thin films by chemical, film electrolytic or plasma-ion bombardment. The etching process removes the material not shielded by the hardened photoresist. Etching is also employed to selectively fashion out patterns such as wires and contact holes once a material has been successfully deposited.

The wet etching method makes use of acid or base solutions. For instance, hydrofluoric acid buffered

with ammonium fluoride is typically used to etch SiO_2.

In recent years, dry or plasma etching has made a lot of inroad. A wafer is placed into the etch tool's processing chamber and given a negative electrical charge [9]. The chamber's temperature is increased to 100°C and brought to a vacuum level of 10 millitorrs, then filled with a positively charged plasma (usually a mix of nitrogen, chlorine and boron trichloride). The opposing electrical charges cause the rapidly moving plasma molecules to align themselves in a vertical direction, forming a microscopic chemical and physical ‘‘sandblasting" action which removes the exposed material. Plasma etching has the advantage of offering a well-defined directionality to the etching action, creating patterns with sharp vertical contours.

Any etch procedure is typified by some properties-profile and selectivity. While the profile describes geometrical shape the film will have after the etching procedure is carried out, selectivity is about the capability of the etch process to differentiate between the layer that is to be etched and the material that is not to be etched. The profile can either be isotropic, in which case, etching occurs at the same pace in both horizontal and vertical directions, oranisotropic, where etching proceeds only in the vertical direction.

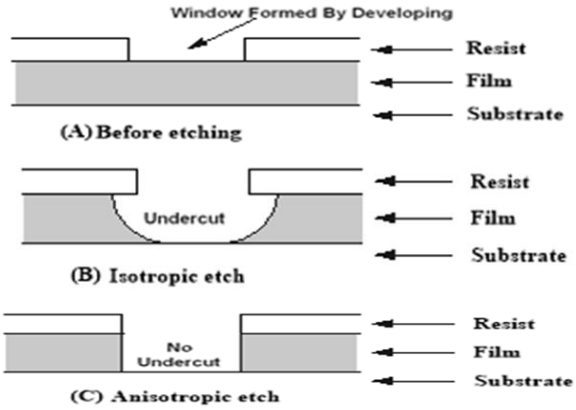


Figure 7(a)-(c) : illustration isotropic and anisotropic etch profiles [10].

VIII. PLANARIZATION

Planarization is a procedure done to smoothen surfaces employing both chemical and mechanical forces. It may be seen as a blend of chemical etching and free abrasive polishing. In order to perfectly deposit a layer of material on the semiconductor surface, it must be ensured that the surface is reasonably flat [11]. If no unique processing steps are taken, this would definitely not be the situation in modern IC manufacturing processes, where multiple patterned metal interconnecting layers are paced over each other. Therefore, a chemical-mechanical planarization(CMP) procedure is involved before the deposition of an additional metal layer on the surface of the insulating SiO_2 layer. This process uses a slurry compound—a liquid carrier with a suspended abrasive component such as aluminium oxide or silica—to microscopically plane the layer of a device and to lower the step heights.

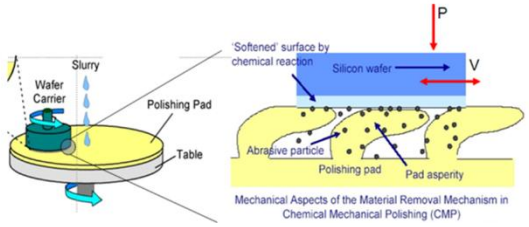


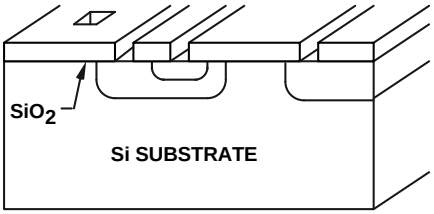
Figure 8: Mechanical Aspects of Material Removal in CMP [12]

IX. METALLIZATION

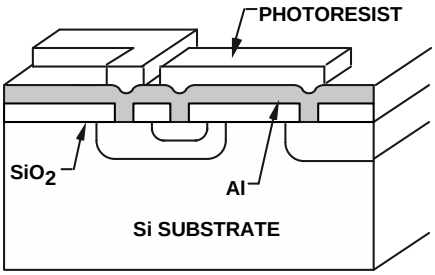
Metallization is the last procedure in the processing sequence of steps involved in the processing of wafer. Metal (usually aluminium or aluminium with a minute quantity of other materials) is used to connect the individual components (diodes, transistors, resistors, and capacitors) in an integrated circuit. A metal layer is deposited on the entire top surface of a wafer. Through photolithography and etch, selected regions of the metal are removed. The remaining aluminium serves as the conductors (wires) between different components of each IC.

The process brings about a thin-film metal layer which will act as the needed conductor outline for the interconnection of the different components on the chip. The metallization process sequence is depicted in Figure(s) 9(a-f). The figures illustrate that an earlier photo-patterning process has removed the silicon dioxide from the areas where ohmic contact will be required. A metal layer is deposited over the

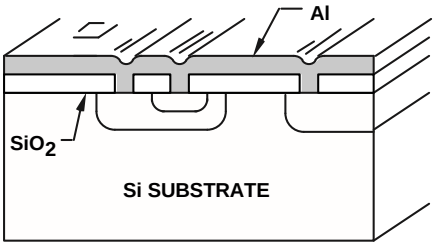
surface and the photo-patterning process is repeated to delineate the metal interconnect.



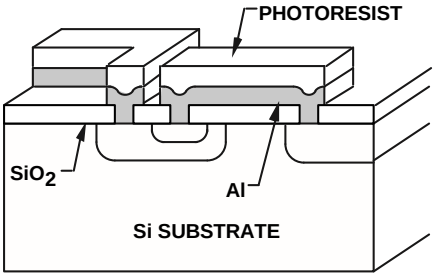
(a) Wafer prepared for Metallization



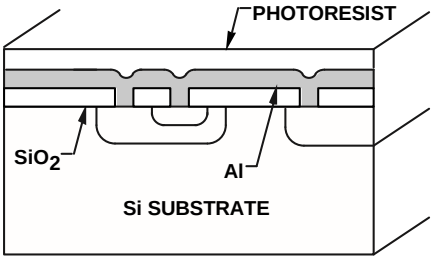
(b) Patterned Photoresist



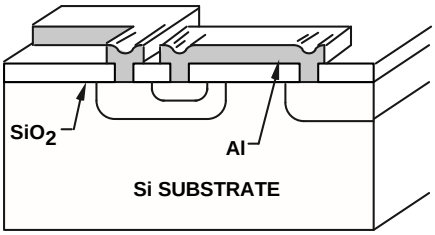
(c) Aluminium deposition



(d) Etched Metallization



(e) Photoresist Coating



(f) Completed Process

Figure(s) 9(a-f): Metallization process sequence [10].

Another purpose of metallization is to form metallized parts known as bonding pads round the border of the chip to form metallized parts for the attachment of wire leads from the package to the chip. The bonding wires are usually 25 micro meters diameter gold wires, and the bonding pads are generally made to be around 100×100 micro meters square to house fully the flat ends of the bonding wires and to give room for some registration flaws in placing the wires on the pads.

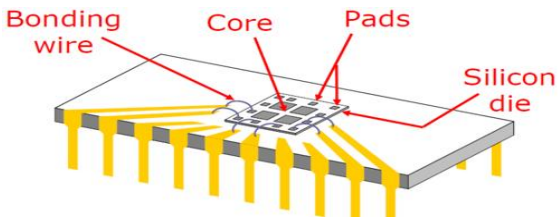


Figure 10(a): A metallized chip [13]

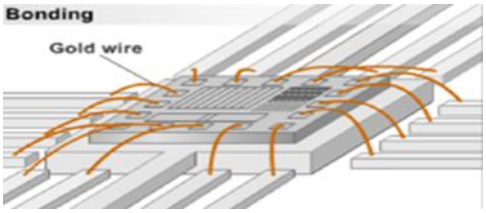


Figure 10(b): The core of a metallized chipShowing bonding wire [13]

After all the wafer making steps which end with metallization have been completed, the good dice within the wafer are ready to be separated and assembled into final product form [13] [14]. The assembly or packaging process will place the electrically good devices (chips, die, and dice are other terms used to identify the individual circuits) in a package, interconnect the device to the package's leads and provide some form of final sealing. As the semiconductor industry advanced from the SSI

(small-scale integration) era through MSI and LSI (medium and large) into the VLSI (very large-scale integration) levels of integration, technology employed in packaging has changed dramatically. The changes have included automation, advances in materials, and new package designs.

CONCLUSION

A detailed sequence of integrating wafers gotten from silicon crystals obtained via the Czochraksi growth process, a crystal growth process that yields high-purity semiconductor, has been carefully outlined in this paper.

The various identified steps are followed methodically to successfully integrate wafers gotten from the Czochraksi growth process. After the last procedure involved in the integration process, metallization, the good dice within the wafer are ready to be separated and assembled into final product form.

REFERENCES

[1] Robert, R.S., IEEE Spectrum archive, 34 (6), p.52-59, 1997

[2] Oyubu, A.O and Okpeki, U.K (2020) Journal of Engineering Studies and Research 26(3), pp 165-172

[3] E. Talik∗ and M. Oboz(2013), Czochralski Method for Crystal Growth of Reactive Intermetallics Acta Physica Polonica A, Vol. 124(2), pp 340-343

[4] Kelemen et al (1958) Method of Melting Silicon, United States Patent Office 3,156,549 Patented Nov. 10, 1964

[5] John Wiley & Sons, Inc M.P Groover, 2002: Fundamentals of modern manufacturing.

[6] http://inst.eecs.berkely.edu

[7] www.circuitstoday.com/chemical-vapour deposition-cvd

[8] https://fenix technico.uliboa.

[9] Federico et al (2004) Silicon Sacrificial Dry Layer Etching (SSLDE) for Free Standing RF MEMS architectures" http://cmi.epl.ch/etch/MEMS03.pdf

[10] Integrated circuit Engineering Corporation

[11] Jeffry J. Sniegowski, (1996) "Chemical-Mechanical Polishing: Enhancing the Manufacturability of MEMS", SPIE Vol. 2879, pp.104-115.

[12] Chien et al, University of California Berkeley, CA:

[13] www.circuitstoday.com/metallization-process

[14] Van Zant, P. (2004): Microchip Fabrication (4th Edition) McGraw-Hill, New York