© SEP 2025 | IRE Journals | Volume 9 Issue 3 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I3-1710972-9609

Amplifier Design for High Frequency in Power Electronics System

SADIQ MUHAMMAD[1], IBRAHIM AKU GODWIN[2]
[1]*Department of Physics , Federal University Brinin-kebbi, Kebbi, Nigeria*
[2]*Department of Physics, Federal University of Technology Minna.*

ABSTRACT- ***The inherent limitation of gain bandwidth products normally presents the need to cascade amplifying circuits but cascading technique always has a drawback of shrinkage bandwidth. A solution to the bandwidth shrinkage was presented using cascode amplifier configuration. Cascode amplifier techniques address the inherent limitation of gain bandwidth. The simulation and analysis of the proposed configuration shows significant improvement on the bandwidth. The overall results of using the amplifier is found to enhance the strength of the transmitted intensity.***

Keyword: Cascode amplifier, cascading.

I. INTRODUCTION

The need for transmitting high power to far distances in the desired direction and improving the receiver sensitivity to any incoming signals increases the number of antenna elements that are used in array antenna systems (Josehph and Malcom, 2001). Each antenna elements need separate feeding structure to control the individual amplitude and the phase. The splitting and recombining of electromagnetic signal is a fundamental signal processing functionality in electronics (Kushwaha and Sirvastava, 2013). As the data rate in a digitally modulated wireless communication system increases, corresponding increase in the output power of the signals radiated by a tower-mounted antenna is typically required by a given service area. (Boylestad and Nashelsky, 2009). Thus, migrating an existing system to a higher data rate often requires more output power from the amplifier used in the system and or a reduction of losses associated with components in the system. There is a higher need to achieve higher data rate which means high frequency carrier and high frequency transmission is limited by the amplifying devices. (Virdee and Virdee, 1999). This amplifying device has the problem of intrinsic gain-bandwidth limitation. High power transmission also require semiconductor that can handle large current and power. The effect of the above limitation is minimized using casode amplifier. The broadband amplifier is a key building block at the transmitting ends in convectional communication circuits. The gain-bandwidth product of broadband amplifier is severely limited by device technology. (Harvey *et al.,* 2000). This amplifying device has inherent limitation of gain – bandwidth products which forced one to compromise the gain at the expense of the bandwidth or vice versa. (Wolf *et a*l.,2005) Circuits with very wide bandwidth are needed in modern communications for efficient high data rate transfer. The design of such circuit is one of the challenges faced in radio frequency receivers. Many amplifier topologies have been proposed so as to satisfy the requirement for gain and bandwidth. Most of the single stage devices in the review could not satisfy the gain and bandwidth requirements as shown in figure 1 below.

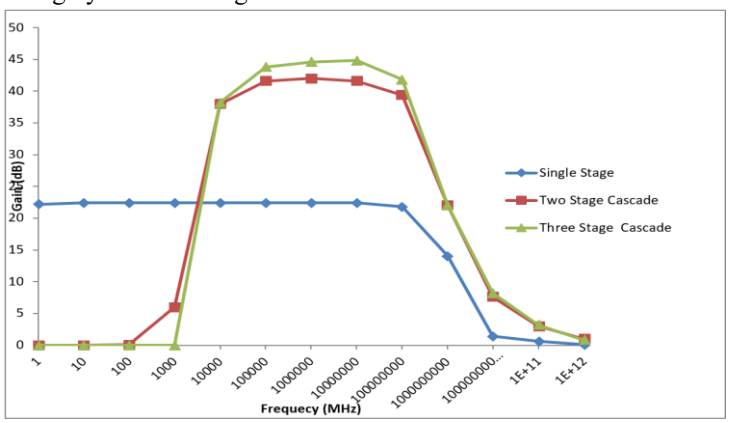

Fig 1 Bandwidth shrinkage.

© SEP 2025 | IRE Journals | Volume 9 Issue 3 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I3-1710972-9609

In this work, we proposed the application of cascode as modifies the bandwidth shrinkage

II. METHODOLOGY

2.1 Design of Amplifier

The three configurations of amplifier were reviewed, the common emitter circuit was found to be the most efficient, due to it high current gain, moderate output to input impedance ration, high voltage and power gain, for this reason a single stage common emitter amplifier was design as shown Fig, 2 below. It was observed that the voltage or power gain from a single state amplifier is limited. Also insufficient for all practical applications, therefore in order to achieve greater voltage and power gain, more than one stage must be used. Such an amplifier is called a multistage amplifier. A multi-stage amplifier was design with common emitter as the first – stage and common base amplifier as the second stage. This form of amplifier is called cascode amplifier.

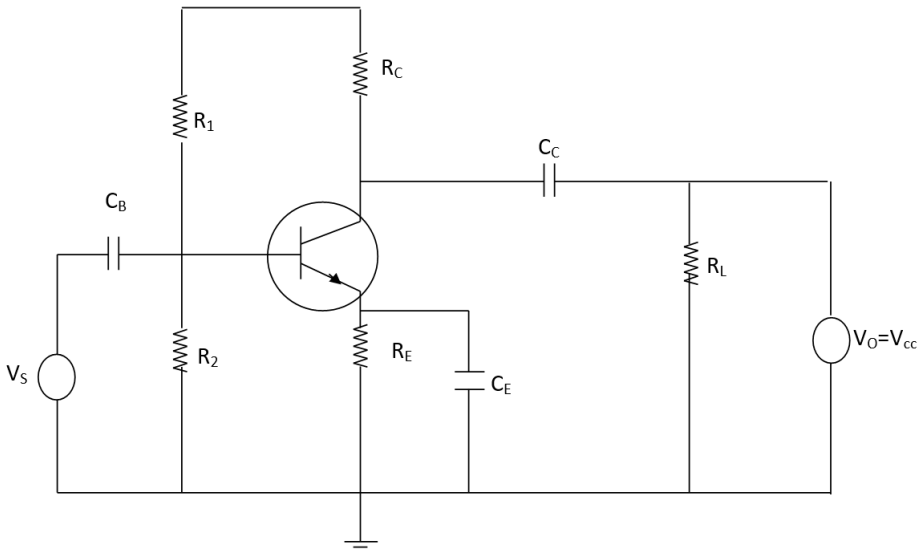

Figure 2: Single stage common emitter amplifier

2.2 Design Equation

Applying Kirchhoff's law to the output and input side of the D.C. equivalent circuit of the figure above we have: (Sedra and Smith, 2004)

$$Vcc = I_C R_C + V_{CE} + I_E R_E \quad (1)$$

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E \quad (2)$$

Thermal stability of the amplifier requires that

$$R_B \leq 0.3BRE \quad (3)$$

and

$$R_E = 0.2R_C \quad (4)$$

The collector emitter current amplification factor is given by

$$B = \frac{I_C}{I_B}$$

and

For $I_E = I_C + I_B$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \quad (5)$$

The bias equation was use to obtain V_{BB} given by

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \quad (6)$$

R_1 and R_2 were determined using R_B and V_{BB} given by the equation

© SEP 2025 | IRE Journals | Volume 9 Issue 3 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I3-1710972-9609

$$R_1 = \frac{V_{CC} R_B}{V_{BB}} \quad (7)$$

$$R_2 = \frac{R_B}{1 - V_{BB}/V_{CC}}$$

or

$$R_2 = \frac{R_B R_1}{R_1 - R_B} \quad (8)$$

The coupling capacitor C and the emitter by pass capacitor C_E were obtained using.

$$f = \frac{1}{2\pi ZC} \quad (9)$$

2.3 Design Equations for Cascode Amplifier

In the design, the same transistors were used in the common emitter and common base stage, hence $\beta_{F1} = \beta_{F2} = \beta_F >> 1$, that is the base current of the transistors is negligible, and base current can be ignored in comparison to the currents through the biasing resistances. Figure 3 below shows the schematic diagram of cascade amplifier. Therefore, the DC biasing base voltages are given by (Dogman and Jenkin, 2010)

$$V_{BB1} = \frac{R_1}{R_1 + R_2 + R_3} V_{CC} \quad (10)$$

$$V_{BB2} = \frac{R_1 + R_2}{R_1 + R_2 + R_3} V_{CC} \quad (11)$$

The Collector and emitter currents is given by,

$$I_{E1} \cong I_{C1} = I_{E2} \cong I_{C2} = \frac{V_{BB1} - V_{BE}}{R_E} \quad (12)$$

The collector emitter voltages are given by

$$V_{CE1} = V_{BB2} - V_{BE2} - (V_{BB1} - V_{BE1}) \quad (13)$$

$$V_{CE2} = V_{BB2} - R_C I_{C2} - (V_{BB2} - V_{BE2}) \quad (14)$$

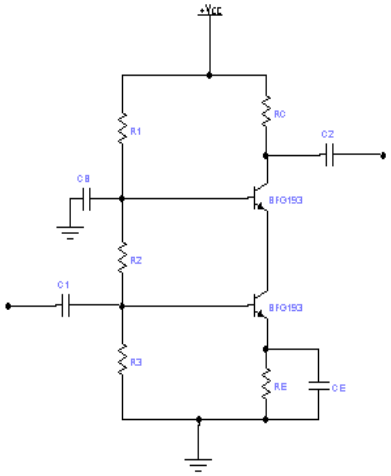

Figure 3: Cascode amplifier

2.4 Analysis of High Frequency Hybrid Π Model

The analysis result was obtained by replacing the transistors in the circuits above with the high frequency Hybrid-πModel of the Bipolar Junction Transistor (BJT). Figure 4 shows the high frequency BJT Hybrid-π Model, by neglecting r_x and r_o we have the small signal equivalent circuit of the 2-configurations as shown in fig. 5.

Were

r_x = Spreading resistance, gmVπ = gmVbe = Ic – equivalent current generator

$r_1 = r_\pi$ =Dynamic emitter resistance, $c_1 = c_\pi$ = Dynamic emitter capacitance

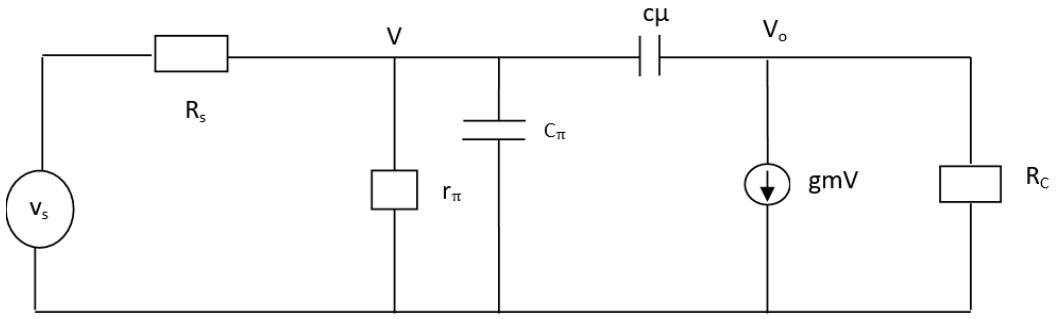

Fig. 4: High frequency common emitter hybrid π – model

© SEP 2025 | IRE Journals | Volume 9 Issue 3 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I3-1710972-9609

At node 1

$$\frac{V-V_S}{R_S}+\frac{V}{Z_\pi}+\frac{V-V_O}{XC\mu}=0 \quad (15)$$

at node 2

$$gmV+\frac{V_O-V}{X_u}+\frac{V_o}{R_c}=0 \quad (16)$$

$$A_V(S)\frac{\mathrm{V_o}}{\mathrm{V_s}}=\frac{G_s r_\pi\left(g_m-SC\mu\right)}{S^2C_\pi C\mu r_\pi+SG_CC_\pi r_\pi SG_C r_\pi C\mu+SG_SC\mu r_\pi+SC\mu r_\pi g_m+SC\mu+G_CG_S r_\pi+G_C} \quad (17)$$

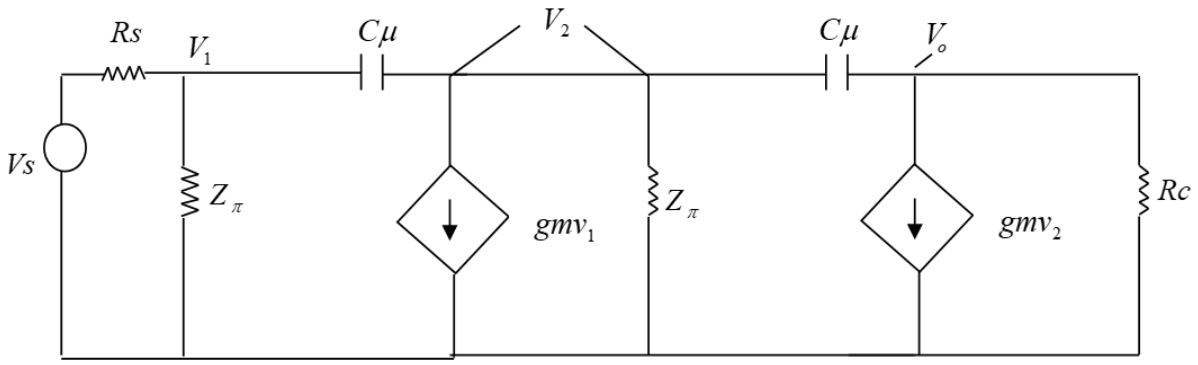

Fig. 5: High frequency cascode hybrid π model

Nodal equation

At V_1 we have

$$\frac{V_1-V_s}{R_s}+\frac{V_1}{Z_\pi}+\frac{V_1-V_2}{X_{cu}}=0. \quad (18)$$

at V_2 we have

$$\frac{V_2-V_1}{X_{Cu}}+gmV_1+\frac{V_2}{Z_\pi}+\frac{V_2-V_0}{X_{Cu}}=0 \quad (19)$$

at V_0 we have

$$\frac{V_0-V_2}{X_{Cu}}+gmV_2+\frac{V_0}{R_C}=0 \quad (20)$$

where

$$\frac{V_0}{V_S}=\frac{G_S\left(r_\pi SCu-gmr_\pi\right)\left(SCu-gm\right)}{\left[\left[SC_\mu+G_C\right]\left[2r_\pi SC_\mu+SC_\pi r_\pi+1\right]-r_\pi SC_\mu\left[SC_\mu-gm\right]\left[r_\pi G_S+1+SC_\mu r_\pi+SC_\pi r_\pi+1\right]-\left[SC_\mu+G_C\right]\left[r_\pi SC_\mu-gmr_\pi\right]\left(SC_\mu r_\pi\right)\right]} \quad (21)$$

III. RESULT AND DISCUSSION

3.1 Design Amplifier

The simulated and calculated result of the 2 – amplifiers configuration are shown. The gain for the simulation was obtain from the plot of voltage gain against frequency, while that of the analysis were obtain form equation 17 of common emitter, and equation 21 of cascode amplifier respectively. And the graphs for the simulation and analysis are shown in the Figures 6 and 7 below.

© SEP 2025 | IRE Journals | Volume 9 Issue 3 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I3-1710972-9609

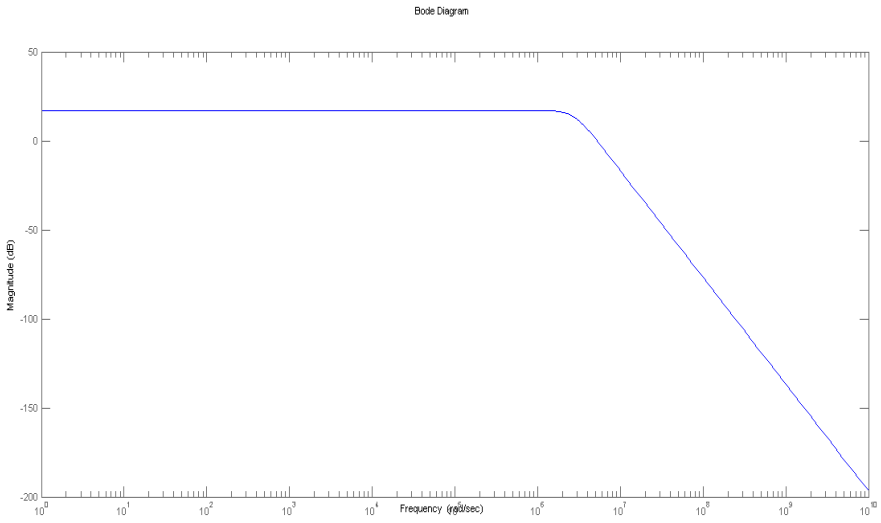

Fig. 6a: Theoretical Frequency Response for Common Emitter Amplifier

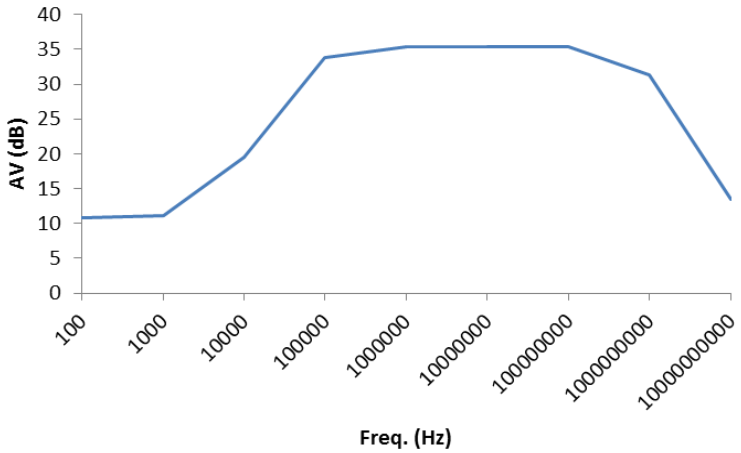

Fig. 6b: Simulated Frequency Response for Common Emitter Amplifier

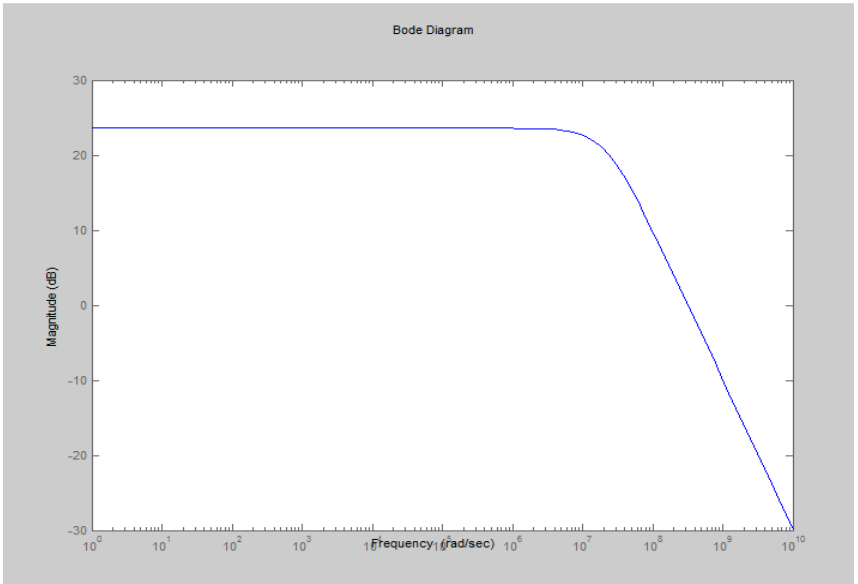

Fig. 7a: Theoretical Frequency Response for Cascode Amplifier

© SEP 2025 | IRE Journals | Volume 9 Issue 3 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I3-1710972-9609

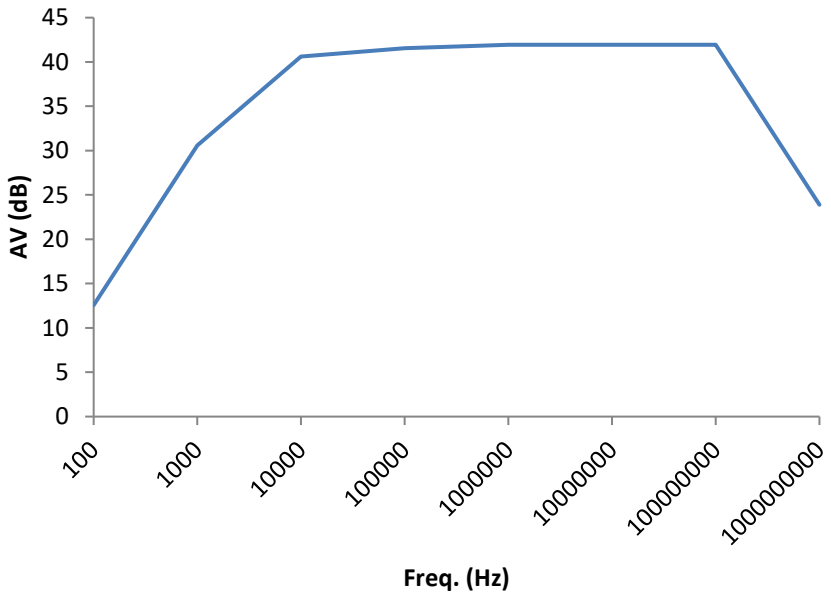

Fig. 7b: Theoretical Frequency Response for Cascode Amplifier

The values of the component used in the design are shown below.

$$R_B = 5.6112\times10^3\Omega,\quad R_1 = 30.0\,ka,\quad R_2 = 6.90\times10^3\Omega$$

$$R_C = 1.34\times10^3\Omega,\quad R_E = 267.22\Omega,\quad C_b = 141pf,\quad C_c = 60pf,\quad C_e = 3\eta f$$

$$C_\pi = 0.15pf,\quad C\mu = 0.55pf,\quad \beta = 70,\quad g_m = 0.112,\quad r_\pi = 6252\Omega$$

$$G_C = 0.00075\Omega,\quad G_S = 0.000182\Omega$$

For the single stage we have

$$A_V(S) = \frac{6.18755\times10^{-14}S - 0.0126}{5.16\times10^{-23}S^2 + 3.9440\times10^{-11}S8.34\times10^{-4}} \tag{22}$$

For the multistage we have

$$A_V(S) = \frac{1.418\times10^{-25}S^2 - 5.775\times10^{-14}S + 5.88\times10^{-3}}{4.028\times10^{-23}S^2 - 2.844\times10^{-21}S^2 - 2.319\times10^{-11}S + 8.344\times10^{-4}} \tag{23}$$

3.2 Discussion

It was found that the cascode amplifier overcome the losses of signal strength in the distributed power amplifier configuration. This work also eliminates the possibility of overheating the circuit board when adequate heat is developed from the insertion losses. Adopting the proposed technique at backhaul location would further reduce cost of handling cooling systems due to heat develop in the circuits from the large currents.

IV. CONCLUSION

In conclusion, it can be seen that the use of cascode amplifiers at the output section eliminate power lose in the circuit and give more chances of enhancing transmitted power of signals compared to the gain-bandwidth restriction present in the amplifying devices.

REFERENCE

[1]. Boylestad, R.L. and Nashelsky, L. (2009). “Electronic Devices and Circuit Thoery”.10th edition. Pearson. PP. 161 – 180.

[2]. Dogman, M. and Jenkins, I. (2010).“A tunable X–Band SIGE HBT Single Stage Cascode LNA”. 11. IEEE Microwave symposium.

[3]. Harvey, J., Brown, E.R. and York, R.A. (2000). “High Power Transmitter”, *IEEE Microwave*, PP. 48 – 50.

[4]. Joseph, M.P. and Malcolm, M.M. (2001).“Electronic amplifier circuit, theory and design”.McGraw-hill book company, Inc. New York. PP. l-6, Pp. l01-120.

[5]. Kushwaha, R.S. and Srivastava, D.K. (2013).“Bandwidth Enhancement of AMicrostrip Patch Antenna with Square Shape Parasitic Elements”. *International Journal of Advanced Research in Computer Science and Software Engineering*.Vol.3(12).

[6]. Sedra, A.S. and Smith, K.C. (2004).“Microelectronics Circuits”.5th edition.Oxford University Press.PP.150-153.

[7]. Virdee, A.S. and Virdee, B.S. (1999)."2 to 18 GHz Ultra-broadband Amplifier Design Using a Cascaded Reactively Terminated Single-stage Distributed Concept*," IEE Electronics Letters,* Vol. 35, PP. 2122-2123.

[8]. Wolf, G., Demichel, S., Leblanc, R., Blache, F., Lefevre, R., Dambrine, G. and Happy, H. (2005). “A Metamorphic GaAs HEMT Distributed Amplifier with 50 GHz Bandwidth and Low Noise for 40 Gbits/s Optical Receivers”. *Institute d’ Electronique de Micro e’lectroniqueet de nanotechnologie (IEMN)* 13th GAAS symposium – Paris.