Building Semiconductor Capabilities in Developing Economies

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Abstract- ***It is not an inaccurate saying that modern industry and scientific progress are largely underpinned by semiconductors. These increasingly nano sized inventions are in fact underestimated in our modern thought and popular culture. Known but barely understood by developing nations and economies, it remains a singular pillar that rests on many years of previous scientific and technological ingenuity that enables our modern world function. The capital intensity, knowledge complexity, geo-strategic pressures of semiconductor manufacturing keep most developing economies on the demand side of the value chain OECD, 2025; Semiconductor Industry Association [SIA], 2025). I seek to analyze in practical and simple terms the interrelationship between semiconductor manufacturing and development challenges; mapping the semiconductor value chain and its possible entry points; the economic, technical, organizational and macro-economic barriers. I seek to propose a staged approach to formulating a strategy for beginning and scaling semiconductor capabilities. I hope that at the end of this analysis, a practical tool kit, risk controls and measurable milestones can be adapted and tailored for beginning or even scaling semiconductor manufacturing participation for resource constrained environments.***

I. INTRODUCTION

Semiconductors are general purpose technologies with economy wide spillovers. For developing nations, participation within the semiconductor value chain can catalyze economic diversification, higher export receipts and productivity along with much needed skill employment pools. However, the sophisticated and deep tech nature of the semiconductor value chain often leaves developing economies on the back end of very high costs, can create steep learning curves and reveal deep infrastructure and resource gaps (U.S. Bureau of Industry and Security [BIS], 2023, 2024; U.S. Government Accountability Office [GAO], 2024).

This analysis will seek to offer a realistic playbook to;

a. start where capability, capital and risk profiles can align.
b. Leverage global partnerships.
c. Gradually expand capability through step by step design, packaging and node manufacturing.
d. Build towards differentiation and drive expertise in niches such as (power, electronics, sensors and specialty processes) (McKinsey & Company, 2023; OECD, 2024).

II. THE SEMICONDUCTOR VALUE CHAIN

The semiconductor value chain can be divided 4 major areas, however with multiple sub divisions under each area

- Design: Often the highest knowledge area where Intellectual property can be realized (Cadence Design Systems, n.d.; EUROPRACTICE, 2025; GlobalFoundries, n.d.). Through Electronic design Automation (EDA), chips can be designed with unique or niche capabilities. This area has the lowest physical capital requirement but can depend on access
- Fabrication (foundry): This area involves the making of the actual chips. This is a capital heavy area. The entrance into leading edge nodes here is very steep and can constitute a significant barrier for new entrants. Mature nodes at 90-65-40-28 nanometer are very complex to manufacture but can be very competitive in today's markets (OECD, 2024; Yole Group, 2024a, 2024b)
- Assembly, Test Marking & Packaging: This area constitutes the final areas of semiconductor manufacturing including the assembly and testing, marking and packing. Here OSAT (Outsourced Semiconductor Assembly and Test) players can be very cost effective. This area is a moderate capex but has a strong job creation argument. It can constitute a strong and pragmatic entry point that is part of an industrial policy (TrendForce, 2025; IEEE Electronics Packaging Society [EPS], 2023a, 2023b).
- Equipment and Materials: These are the equipment and materials used in the manufacture of these complex semiconductors, which are in themselves arguably more complex.

Lithography machines, photoresists, wafer inspection systems, die bonders, specialty gases, etc. are a few examples of the flurry of machines and materials used. This is a very high complexity area; however very viable niches exist. This area can constitute a large competitive advantage. (SEMI, 2025a, 2025b, 2025c; OECD, 2025)

III.STRATEGIC ENTRY PATHS FOR DEVELOPING ECONOMIES

a) Design-Led Path: This area can involve the least cost; examples include fabless chip design for regional applications. (McKinsey & Company, 2023; SIA, 2024a, 2025). These can be semiconductors for automotive micro-controllers, smart cards, IOT sensors, power management devices which could range between 90-22nm. EDA machines can help scale this path in a very effective way.

The advantages here could include fastest capability accumulation; in other words, this area can help build talent in a less time consuming way that would later support manufacturing. Additionally, these can be scaled within university research programs with possible partnerships with mature node foundries. This is a path that could be scaled in and around of 2 to 3 years with the right support

b) OSAT/Assembly Test Marking Packaging: The focus here is assembly and test for a diversity or focused set of semiconductors for Microcontroller units, RF, power devices or analog devices, etc. (TransForce, 2025; EPS, 2023b). Marking and packaging can also be scaled incrementally. This area as mentioned earlier is of moderate capex that is between design and mature node fabrication. It has strong employment metrics and can fit manufacturing clusters. Industrial parks with vendor agreements for handlers and probers is a viable entry point for serious ambitions within the semiconductor space. E.g. The Youngin Semiconductor cluster in South Korea

c) Specialty/Mature-Node Foundry Path: This path is advanced and can constitute the most investment within the semiconductor value chain. However, if achieved can constitute one of the highest competitive advantages in modern manufacturing. There is high demand in the market for advanced foundries with increasing complexity

IV.INFRASTRUCTURE REQUIREMENTS AND TECHNICAL BASELINE

- Facilities such as clean rooms with ISO certifications ranges depending on the process are critical facility requirements. Bulk specialty gases and ultra-pure water plants together with uninterrupted power are non-negotiable (ISO, 2015; Semiconductor Engineering, 2025; WEF, 2024).
- Tools for Assembly Test Marking and Packaging such as die attachers, wire bonders, X-ray, ATE testers and reliability labs constitute critical must-haves for the ATMP stage (EPS, 2023b). It gets more sophisticated for Mature foundries where Lithography (I-line/DUV) machines, diffusion/implant CMP, defect inspection machines, etc. (OECD, 2024; SEMI, 2025a, 2025b) are required components of the manufacturing line.
- Process and Quality Systems: The level of accuracy, cleanliness and manufacturing precision required mandates the adoption of thorough equipment maintenance schedules, e.g. six-sigma principles, clean room protocols and major ISO certifications (IATF Global Oversight, n.d.; EPS, 2023a).
- Software requirements such as EDAs yield analytic software are important.
- Talent and Training: Technician pipelines, co-op programs, vendor certified maintenance tracks, returning diaspora incentives are highly required (SIA, 2024a, 2025; OECD, 2025).

V.DEVELOPMENT CONSTRAINTS

Many developing nations are not only resource constrained but can have low experience on the coordination and sophistication private and public stakeholders within this sector need to have to deliver on tangible results. Let us look at them by category

Technical and industrial

- Extreme precision equipment and requirements such as lithography machines UP gases, clean room standards can be very cost prohibitive. (International Organization for Standardization [ISO], 2015; Semiconductor Engineering, 2025; World Economic Forum [WEF], 2024)
- Talent bottlenecks across design and process integration steps can pose a challenge. Talent

around equipment maintenance is very specialized as such the pool may be small
- Supply chain dependency on a small group of countries constitute technical as well as political hurdles

Organizational and Governance
- Fragmented and siloed agencies can constitute slow permitting processes. Custom delays for sensitive equipment can elongate deadlines and slow timelines (OECD, 2025)
- Weak Intellectual Property regimes will not engender trust from suppliers and could weaken already limited vendor relationships
- Inadequate university – industry linkages will reduce problem solving time and weaken mission driven objectives

Macroeconomic
- A lot of developing nations face currency volatility especially when most global contracts are denominated in reserve currencies such as USD/EUR. (Reuters, 2025; WEF, 2024)
- Weakened power grid access, water stress, logistics friction, country risk perceptions are a few of the significant barriers developing nations may be battling with when intending to scale in this sector

VI.SUGGESTED ECONOMIC AND POLICY INSTRUMENTS

For developing jurisdictions, focused and administration agnostic policy instruments need to be employed for a sustained development within the sector. Some of them are Semiconductor Mission Office (SMO): Creating a semiconductor mission or development office as a single window authority that has full legal backing is critical (OECD, 2025). This office should have its own budget with procurement powers and an export compliance program. The board of SMO must be a multi-discipline, multi-stakeholder board immune to political interference.

Incentives: The scale and sophistication of incentives have a direct impact on the growth and development of this sector. Time bound subsidies for capex on equipment, result based grants tied to yield, accelerated depreciation tariffs and/or VAT waivers for tools can help drive proliferation of stakeholders and accelerate results within the sector (World Bank, 2025; McKinsey & Company, 2023). This section is not exhaustive, but stakeholders must be consulted to determine the best type of incentives that would suit the particular strategy and specialization

Finance: Due to significant cost structures, the financial frameworks must be targeted at making accessing finance frictionless for those that qualify. Sovereign co-investment JV with vendors can deploy capital to experts for rapid set up. Development bank credit lines are important for low interest financing access. Even revenue sharing formulas for tool and equipment providers can help reduce barriers for equipment access.

Intellectual Property and Standards: Creation and fast track timelines for judgments on IP courts can help engender trust with stakeholders. Adherence to JEDEC/IPC standards are critical. Data protection MOUs with foreign partners create a foundation of trust and a framework for attraction of more partners (SIA, 2024b; OECD, 2025)

Trade Infrastructure: Creating custom trader lanes with customs pre-clearance for controlled items is a practical and suggested tactic for fast-tracking the trade and logistics element

Demand Creation: Suggested procurement policies by the public sector can enable off-take numbers for locally produced and packaged power controllers, microcontrollers for IOT devices. Roadshows can also be supported.

VII.ORGANIZATIONAL SETUP AND GOVERNANCE

Special Purpose Vehicle: Agreements with professional operators is a major first step for squaring the needed know how and organizational expertise for this enterprise. This SPV must be separated from political cycles (OECD, 2025)

Programs Portfolio: it is important that organizational programs are designed as frameworks for the development of the sector. Suggested programs could be Design Catalysts on EDA software. Testing and Marking Accelerators with industrial clusters and universities. Beginning Supplier localization programs. Workforce academies for upskilling in semiconductor disciplines.

Procurement and Vendor Management: Long term framework agreements with tool and machinery vendors are important to sustain supply and maintenance schedules (Cadence Design Systems, n.d.; SEMI, 2025b).

Risk and Compliance: For a semiconductor industry to thrive, some level of export controls must be put in place. Now this is where jurisdictions need to be careful not to trigger retaliatory measures. However there must be the funneling of critical materials that are required within the semiconductor industry into limited ship-out lists. For the sole reason that it is required and would be needed to build out a sustainable supply chain. Supply Chain traceability frameworks must also be implemented and end-use screening for procurement of certain minerals will keep a jurisdiction on top of its supply chain. Cybersecurity is also important as a component of IP protection (BIS, 2023, 2024; GAO, 2024).

VIII.SUGGESTED PHASED ROADMAP

1. Phase 1 - (0-3years)
    a. Launch the EDA Cloud with subsidized access for over 100-200 design startups and universities
    b. Establish Semiconductor Mission/Development Office and talent academies. Diaspora programs are key to attract talent within established industries
    c. Establish and set up Assembly Test, Marking and Packaging lines in a dedicated industrial park and infuse certifications and standards such as the IATF 16949 certification
    d. PDK (Process Design Kits) are very important, so signing MOUs with established foundries for access to PDKs will be very important. Making the access subsidized for design teams will be critical in helping build up capabilities. (Cadence Design Systems, n.d. [#9]; EUROPRACTICE, 2025; IATF Global Oversight, n.d.; SIA, 2024a).

2. Phase 2 – (Years 2 – 5)
    a. With the design expertise maturing, expanding into more complex packaging lines with reliability labs is key. The idea is that with testing and assembly beginning to become more mature, teams will begin to notice problems and solve for them. They will need the tools for this.
    b. Commission more specialty device lines like Silicon Carbide (SiC) semiconductors for electric vehicles power electronics. This will geometrically improve the expertise for more advanced chipsets and chiplets (Yole Group, 2024a, 2024b; Holland & IEEE EPS HIR Working Group, 2024).
    c. Secure anchor customers with offtake contracts and integrate with local electronic supply chains. Look for leading importers into the country with the aim of being part of their materials mix.

3. Phase 3 (Years 5-10)
    a. Advancing to 2.5D packaging and chipsets with global partners is essential. South Korea is the 1980's focused on DRAM (Dynamic Random Access Memory semiconductors market learning from Japanese and American manufacturers to carve out a niche and expertise by the 1990s (chiplets/2.5D) via partnerships (IEEE EPS, 2023a; SEMI, 2025c; OECD, 2025).
    b. Add 200mm foundry to expand specialty processes and to deepen supplier base. Move toward a regional hub status.

IX.POLICY TOOLKIT

Regulatory and Business Policy

Some of the suggested policy frameworks have been alluded to earlier in this analysis, but for the sake of succinctly describing them

- Semiconductor specific custom lanes must be prioritized; 48-72 hour equipment clearance policy should be adopted. (WTO, n.d.; OECD, 2025; SIA, 2024b).
- IP fast track courts to secure design and data regulation
- Standards must be strictly enforced as a way of enshrining trust within the industry and securing ready markets

Incentive and Finance

- Up to 50% capex share is suggested especially for first movers. This can be implemented with a declining schedule in order to make set up rapid. Energy price guarantees should be implemented as a way to secure energy reliability.
- Outcome based grants should be implemented

Workforce

- National Curriculum for Semiconductor Engineering should be enacted with specific disciplines in Yield, Process and test engineering. There should be 1-2 year diplomas led or sponsored by vendor partners or perhaps even taught by vendors. Certifications should also be adopted or established (SIA, 2024a, 2025).

Security and Compliance

- There should be an export-compliance unit within the SMO. Cybersecurity standards for EDA software, multi-sourcing for critical chemicals should be prioritized to hedge against shortages and political issues around supply (BIS, 2024; U.S. GAO, 2024).

Sustainability

- Semiconductor foundries use a lot of water, as such Ultra-Pure Water reclaim targets should be enacted to enable sustainable operations of foundries. Renewable power purchase agreements can also be baked into the policy formulation (Semiconductor Engineering, 2025; WEF, 2024).

X.MONITORING AND EVALUATION (KPIs)

Capability: Number of certifications achieved by ATMP lines. Number of tape-outs (Design completions)

Economics: The amount of yield (number of functional vs defective chips) is a critical success factor in any fabrication initiative for semiconductors. This is a KPI that will enable assessment of all the input effort and processes used in design manufacture and packaging.

Ecosystem: The number of suppliers that have been onshored or localized is a key metric. The number of research outputs translated into products is also another key metric

Sustainability: Water recycling levels, renewable energy use, audit pass rates and incident free operations are key metrics that should be incorporated into the sustainability KPI. (IATF Global Oversight, n.d.; ISO, 2015; EPS, 2023a).

CONCLUSION

For developing nations, the path to semiconductors is not a binary choice between irrelevance and chasing the leading edge. A sequenced niche oriented strategy can create durable capabilities and economic spillovers. Success depends on focused governance, credible partnership arrangements, dependable infrastructure, protected IP, patient and patient capital among many others (OECD, 2025; BIS, 2024; GAO, 2024; SIA, 2025). With these in place semiconductor manufacturing can become a realistic engine of industrial upgrading rather than an aspirational slogan

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