© OCT 2025 | IRE Journals | Volume 9 Issue 4 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I4-1711457-8358

Design and Simulation of a Miniaturized CMOS Compatible Coplanar Waveguide Bandpass Filter for 5G Millimetre-wave Application

BELLO O. LAWAL[1], CHEAB SOVUTHY[2], ISAH M. M[3]
[1] *Department of Computer Engineering, Edo State University Iyamho*
[2] *Department of Electrical Electronic Engineering, University Teknologi PETRONAS*
[3] *Department of Computer Engineering, Edo State University Iyamho*

Abstract- ***The current CMOS millimetre-wave filters are implemented using microstrip technology. Thus, they are characterised by high losses due to parasitic effects and large-distributed capacitance resulting from coupling effects. We present the design of a miniaturised CMOS compatible coplanar waveguide bandpass filter for a 5G millimetre-wave application. The bandpass filter consists of a third order Combline structure loaded with interdigitated capacitors and a coplanar ground plane. The miniaturised bandpass filter is theoretically modelled and simulated for compatibility with the standard CMOS process technology to significantly reduce design complexity, to achieve a high-performance filter with minimised signal losses of insertion loss (IL) less than 2dB, return loss (RL) better than 10 dB, with good selectivity, low cost, compact size, low weight, and high linearity. The theoretical parameters of the bandpass filter are calculated using MAPLE software based on mathematical modelling equations of Combline structure and the ideal transmission line schematic model in ADS used to predict the performance of the filter. The CMOS process technology due to its high monolithic integration level and low-cost implementation for batch fabrication makes it a good candidate for achieving low cost and high-performance filter. The theoretical and ideal schematic model results of the miniaturised CMOS bandpass filter show an insertion loss of 0dB and return loss better than 20 dB at 60 GHz. The filter is simulated for compatibility with the standard 0.18µm CMOS process technology using HFSS finite element analysis (FEA) to confirm its performance. The simulated result obtained for a single metal layer of the miniaturised bandpass filter shows an insertion loss of 0.03 dB, return loss better than 29 dB at a centre frequency of 60 GHz and occupy a total chip area of the 580.6 µm x 334.7 µm with a core size of 400.6 µm x 127.7 µm. While the optimised three metal layers model with CMOS design rules consideration shows an insertion loss of 0.45 dB and return loss better than 10.8 dB at 60 GHz with a core size of 439.6 µm x 127.7 µm. Abstract- Mention the abstract for the article. An abstract is a brief summary of a research article, thesis, review, conference proceeding or any in-depth analysis of a particular subject or discipline, and is often used to help the reader quickly ascertain the paper's purpose. When used, an abstract always appears at the beginning of a manuscript, acting as the point-of-entry for any given scientific paper or patent application.***

Index Terms: Coplanar waveguide, Bandpass, 5G, Combline, CMOS.

I. INTRODUCTION

The advent of the fifth generation (5G) mobile communication has led to an increased interest in millimetre-wave technology [1-3]. The 60 GHz unlicensed millimetre-wave frequency band is a band of frequency suited for 5G applications and a promising solution for next-generation wireless communication [4, 5]. To realise superior system performance at this frequency, bandpass filters play crucial roles in selecting the fundamental frequency while rejecting other spurious frequencies or harmonics [6]. Consequently, the need for more efficient, low-power, and high-performance, miniaturised filters characterised by low loss and compact form factors have also increased drastically in the last few years [7]. The realisation and application of such miniaturised or compact filters in the front-end transceiver architecture in modern communication systems will facilitate better system design integration with small size, low weight, and low cost [8]. Therefore, these filters need to achieve high performance in terms of low insertion loss, high integration flexibility, compact or miniaturised in size, and most importantly, must be low-cost [9]. Literature in the last decade have revealed different filter technologies for 60 GHz millimetre wave application such as the standard printed circuit board (PCB) technology [10], low temperature cofired ceramics (LTCC) technology [11], flexible organic material-based filter technology [12, 13], and bipolar complementary metal oxide semiconductor

chips. However, there are two most outstanding filter solutions at the 60 GHz millimetre wave frequency. The filter-in-package requires the filter to be implemented in the packaging platform and the filter-on-chip which is structured to achieve miniaturised and compact size with significantly reduced packaging cost [14], [15]. The on-chip bandpass filter implemented in CMOS has gained research attention in the last decade [16-20]. For superior performance, it is ultimately required to minimize the filter design and fabrication complexities, the on-chip physical dimension of the filter, considering the fabrication cost. Based on this design constraint, an innovative design approach to miniaturize the bandpass filter have been presented in the literature using the CMOS process technology [18, 21-23].

The interest in miniaturisation and lightweight components is streaming down the design chain of millimetre wave system in terms of size, weight and power (SWaP) [7]. In the design, space will come at a higher cost than expected with a size footprint. Considering the significance of reducing millimetre wave filter size to stay on top of the overall trend of device scaling down, manufacturing resilience likewise plays a vital role. The recent development in process technology, CMOS process for microwave and millimetre-wave applications has made the design of highly integrated system-on-chip (SoC) both possible and cheap [24]. In the last decade, this technology has gained widespread interest among integrated circuit designers and researchers in designing compact and highly miniaturised bandpass filters, with enhanced performance, used in the front-end transceiver circuits in many wireless communication systems such as mobile phones and wireless local area networks (WLANs) [25].

The recent trend in the 60 GHz millimetre-wave technology band has opened new opportunities for circuit and communication system designers over the last decade. This band provides numerous opportunities for aggregating carrier frequencies that deliver high data rates, in the region of tens of gigabits per second for various applications. Millimetre-wave based bandpass filters have been designed using various planar transmission line structures [5, 6]. However, most of the existing bandpass filters are designed using microstrip technology [6, 9, 26]. Though this technology has been reported and used in most filters design, the filters are characterised by various drawbacks which makes them quite lossy and needing improvement for application in 5G millimetre wave systems [19, 21, 27-37]. They are quite lossy due to the parasitic effect associated with the via holes interconnect and the large distributed capacitive coupling between the top conductors and the ground plane which also leads to poor selectivity. In [27], Hsu et.al designed a 60 GHz millimetre-wave RFIC on-chip bandpass filter. The filter occupied a chip size of 1.148 by 1.49 mm^2. The filter was characterised by investigating the variation in the insertion loss and the bandwidth using different sizes of perturbation stub with a 3 dB bandwidth of about 12 GHz. The filter has a poor insertion loss of 4.9dB and a return loss of 10dB in the passband. In [28], Yang et al. utilised a rectangular open-loop structure to design and fabricate an on-chip second-order bandpass filter on a solid defected ground plane with a die size of 415.5 by 502.8 μm^2. The response shows double transmission zeros at finite frequencies in the stopband giving the filter a good selectivity with an insertion loss of 1.5 dB. When compared to other filters, it is found to be a high-performance filter with low insertion loss, compact in size, good selectivity but with a poor return loss of 9.2 dB. In [21], Yeh et al utilised a six-layer CMOS based millimetre wave conductor-backed half-wavelength resonators to archive a stopband characteristic of the filter at required resonance frequencies. The filter structure which occupies a chip size of 0.225 × 0.55 mm^2 was designed on structural layer M6 while M5 was used for grounding. Though the filter is very compact, however, it has a relatively high insertion loss of 5 dB due to parasitic and distributed coupling capacitive effects between the structural layer and the grounding. In [29], R. K. Pokharel et al. used an enhanced on-chip folded open-loop resonator bandpass filter with a patterned ground shield for 60 GHz millimetre-wave application implemented on a standard CMOS 0.18 μm process technology. The filter has a compact size of 910 × 650 μm^2 with a transmission zero which results in high selectivity. However, the filter is still lossy with an insertion loss of 2.77 dB. In [38], Y.-M. Chen et. al introduced a miniaturised CMOS bandpass filter using open resonators loaded with two grounding pads stepped-impedance stubs to improve the band selectivity and decrease the chip size appropriate for on-chip integration with an RF transmitter and receiver circuit. The grounding pad is built from the

vertical interconnect of the various metal layers of the CMOS process with the end goal that the slow-wave impact is available when inserting it underneath the microstrip signal strip. The compact filter die size of 0.31 × 0.26 mm^2 has a significantly improve selectivity but, however, characterised by high insertion loss of 3.9 dB. In [22] K. Ma et. al. implemented a sandwich quasi-elliptical capacitor in the design of a 60 GHz on-chip multimode bandpass filter. The implementation of the loaded sandwich capacitor shows the capability of multimode perturbation as well as regulating the stopband in the designed bandpass filter. Two transmission zeros generated by the magnetic coupling path further enhance the stopband rejection. The filter shows a size of 0.16 mm^2 with a lossy insertion loss of 5 dB. In 2014 [30], Yeh et. al utilized stepped-impedance resonators in the design of a highly miniaturised bandpass filter taken into consideration more flexibility to control the design parameters and create two transmission zeros by a two-way mechanism which are located at finite frequencies of 32 GHz and 109 GHz and the band-edge selectivity is significantly better with low-insertion loss of less than 2.9 dB and size of 182 × 393 μm^2. In [31], Barakat et al. adopted open-loop microstrip resonators for a miniaturized millimetre wave, low loss CMOS on-chip bandpass filter. The overlapping of the open loop resonator enhanced the resonators intercoupling configuration. The insertion loss of 2.85 dB and return loss of 18 dB at 59 GHz with a bandwidth of 15.5 GHz performance was enhanced by implementing the H-shaped defected ground plane to improve the stopband rejection. The total chip size of the filter was found to be 368 µm × 262 µm.

In this paper, we present the design of a miniaturised 60 GHz millimetre-wave CMOS compatible Combline bandpass filter for 5G application based on the 0.18 µm CMOS process technology using a coplanar waveguide to achieve high-performance systems with minimised signal losses of insertion loss (IL) less than 2 dB, return loss (RL) better than 10 dB, with good selectivity and compact size. The aim is to present a comprehensive design analysis, development, and optimization of miniaturized bandpass filter for 5G millimetre wave application. The coplanar (modified microstrip) structure is used to eliminate the parasitic and coupling effects that cause losses in the conventional microstrip bandpass filters. In section 2, we present the synthesis of the miniaturised Combline bandpass filter with loaded interdigitated capacitors using the appropriate mathematical equations to determine the filter order, selectivity, 3 dB bandwidth based on the computed external quality factor and coupling coefficients, impedance characteristic, effective permittivity, and the physical dimensions of the filter (resonator length, tapping points and width) using MAPLE to optimize the design. In Section 3, the implementation and performance of the optimized bandpass filter in terms of s-parameters by simulation using electromagnetic simulation software tools; High-Frequency Structural Simulator (HFSS) for the miniaturised design compatible with the 0.18 µm CMOS process technology is presented. Section 4 design rule (DRC) and physical verification check (PVC) of the simulated miniaturised bandpass filter for physical violations and compatibility check based on the 0.18 µm process, are presented. Lastly, Section 5 concludes the manuscript.

II. SYNTHESIS OF THE BANDPASS FILTER

The filter design process starts with the filter specification that meets the required performance. These include the filter type, the response type, the order of the filter, the passband rippled that is allowed, the desired operating frequency for its application, passband or stopband range, the maximum attenuation allowed for equal ripple, quality factor (Q_f), the bandwidth (BW), the required insertion loss (IL) and return loss (RL) characteristics. A good approach to designing a practical bandpass filter is to select a lowpass prototype of series (inductors) and shunt (capacitors) components, determine component values and then the component transformation from lowpass to a bandpass. The methodology is shown in Figure 1.

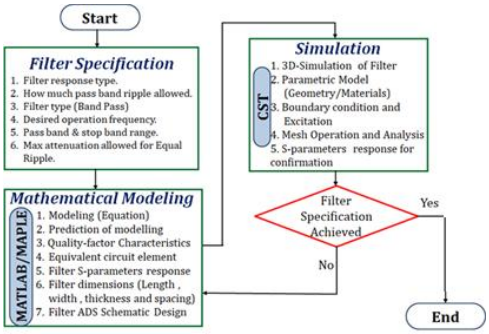

Figure 1: Design methodology flow chart.

© OCT 2025 | IRE Journals | Volume 9 Issue 4 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I4-1711457-8358

A. Design Specification

Figure 2 shows the various components of the proposed bandpass filter. It consists of a third order Combline resonators of electrical length of 50° shunted at one end to the ground and loaded with interdigital capacitors on the other end before shunted to the ground with two tapped feed lines for RF input and output, respectively.

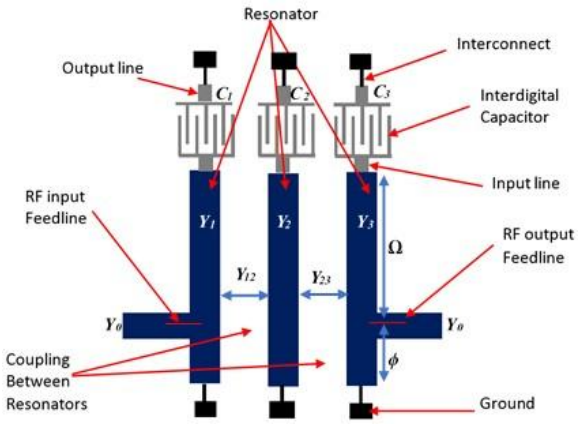

Figure 2: Components of a Combline bandpass filter.

The physical dimensions of length L, width W, and the thickness T of the conductors for accurately designing the combline filter are determined by theoretical modelling and design rules specifications. Table 1 shows the filter design specifications.

Table 1: Design Specification of The Bandpass Filter

Symbol	Parameters	Values
f_0	Centre frequency	60 GHZ
f_1	Lower frequency	57 GHz
f_2	Upper frequency	63 GHz
BW	Bandwidth	6 GHz
IL	Insertion Loss	2 dB
L_R	Return Loss	10 dB
L_A	Stopband Attenuation	40 dB
Chebyshev	Response type	-
θ	Electrical Length	50°
N	Filter order	3
Capacitor	Interdigitated	-
Technology	CMOS	0.18 µm

B. Lowpass Prototype Filter

The low pass prototype is realised from lumped elements g_1, g_2 and g_3 representing the capacitance of a shunt capacitor, and inductance of a series inductor for $N = 3$, where N is the filter order. The values of g_0 *and* g_{n+1} represent the source generator and load impedance. For a lowpass prototype, the g_i values are normalized to give $g_0 = 1$ ohm and the cut-off frequency $\omega_c = 1rad/s$ and are determined using the equation given in [39, 40]. Figure 3 shows a low pass prototype filter of the proposed 3rd order filter.

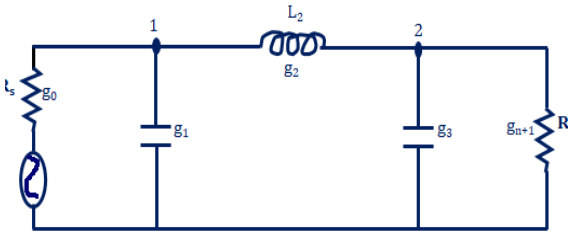

Figure 3: 3rd order low pass prototype filter

C. Replacement of Lowpass Series Element

To replace the series element, a 90° phase-shifting networks of admittance K inverters is used to replace the series inductor by its equivalent circuit. Thus, the series lumped inductor is replaced by its equivalent circuit of a shunt capacitor with two K inverters as shown in Figure 4.

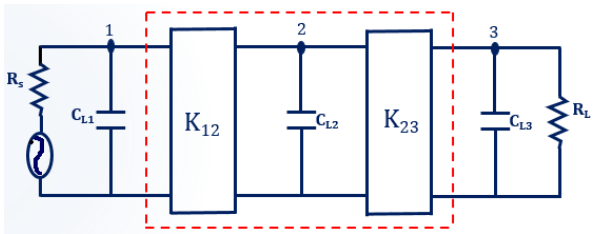

Figure 4: Low pass prototype filter with admittance *K*-inverters

The equations relating the g element values of the lowpass prototype to the impedance K-inverter prototype is given by (1), (2) and (3) [40].

$$\frac{K_{01}}{Z_o} = \sqrt{\frac{\pi FBW}{2g_0 g_1}} \tag{1}$$

$$\frac{K_{i,i+1}}{Z_o} = \frac{\pi FBW}{\sqrt{g_i g_{i+1}}}; \qquad i = 1, 2, \ldots\ldots N\text{-}1 \tag{2}$$

$$\frac{K_{N,N+1}}{Z_o} = \sqrt{\frac{\pi FBW}{2g_N g_{N+1}}} \tag{3}$$

K_{12} and K_{23} are the impedance K inverter values between node 1 and 2; and node 2 and 3. The shunt capacitors (capacitances) values C_{L1}, C_{L2} and C_{L3} are the resulting capacitance values given by (4) [42, 43].

$$C_{Lr} = \frac{2}{\eta}\sin\left[\frac{(2r-1)\pi}{2N}\right] \quad r = 1, \ldots\ldots N \tag{4}$$

D. Scaling and Transformation to Bandpass

To realize a bandpass filter derived from a lowpass prototype filter, the lowpass filter is transformed to bandpass by scaling and transformation process applied to the lowpass prototype filter with normalised element values and cut-off frequency to converted it to a bandpass filter with the desired operating centre frequency and bandwidth. The lowpass filter lower (ω = -1) and upper (ω = +1) band edge frequencies are mapped into the bandpass lower (ω_1) and upper (ω_2) band edge frequencies. The mid-band frequency of the lowpass prototype at ω = 0 is mapped into the centre frequency in the passband of the bandpass filter. The transmission zeros of the lowpass prototype at infinity now occur at both ω = 0 and ω = ∞. The frequency transformation is achieved by using (5), (6), and (7) [44, 45].

$$\omega' = \frac{1}{FBW}\left(\frac{\omega_u}{\omega_0} - \frac{\omega_0}{\omega_u}\right) \tag{5}$$

$$FBW = \frac{\omega_2 - \omega_1}{\omega_0} \tag{6}$$

$$\omega_0 = \sqrt{\omega_1 \omega_2} \tag{7}$$

Where ω_0 represents the centre angular frequency, FBW denotes the fractional bandwidth, ω' represents the normalised frequency of the lowpass prototype and ω_u is the frequency at which minimum cut-off must be achieved (upper rejection frequency). The resulting bandpass filter with parallel resonators of elements L_p and C_p is shown in Figure 5.

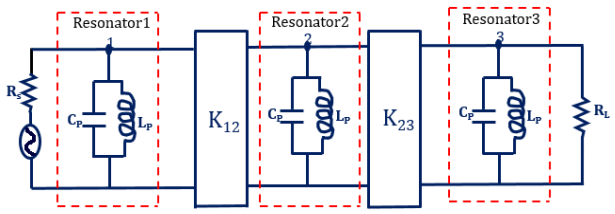

Figure 5: Transformation of lowpass to a bandpass filter

The resulting element values of the parallel LC resonators in the BPF with the impedance scaling taking into consideration are given by (8) and (9) [44, 45]

$$C_p = \left(\frac{\omega_c}{FBW\,\omega_0}\right)\left(\frac{g_i}{\gamma_0}\right) \tag{8}$$

$$L_p = \left(\frac{FBW}{\omega_0 \omega_c}\right)\left(\frac{\gamma_0}{g_i}\right) \tag{9}$$

Where $\gamma_0 = Z_o/g_0$ is the impedance scaling factor, g_i is the i^{th} lowpass element value and ω_c is the lowpass prototype filter cut-off frequency. The bandwidth scaling factor, alpha α and the propagation constant beta β are calculated using (10) and (11) respectively [43].

$$\alpha = \frac{2\omega_0 \tan(\theta_0)}{\Delta\omega\left(\tan(\theta_0) + \theta_0\left(1 + \tan(\theta_0)^2\right)\right)} \tag{10}$$

$$\beta = \frac{1}{\omega_0 \tan(\theta_0)} = \frac{C}{Y_{rr}} \tag{11}$$

where θ_o is the electrical length of the Combline resonator. The C is the capacitance of the Combline bandpass filter and Y_r is the admittance of the r^{th} resonator. The ω_o and $\Delta\omega$ values are given by (12) and (13) [43].

$$\omega_o = 2\pi f_o \tag{12}$$

$$\Delta\omega = 2\pi\Delta f \tag{13}$$

E. Determination of Resonators Admittances

The Combline structure is a distributed structure that consists of an array of coupled resonators with coupling between adjacent resonators. The shunted resonators with electrical length θ_o, ϕ is the length from the shunt end of the resonator to the ground and the tapped point, $\Omega = \theta - \phi$ is the length from the tapped point to the end of the resonator before the loaded capacitor, C_1, C_2 and C_3 are the loaded capacitors for each resonator, Y_1, Y_2 and Y_3 are the resonators line admittances, y_{12} and y_{23} are the characteristic admittances of the series shorted stubs between the resonators. Y_0 is the characteristic admittance of the Combline. The distributed resonator model equivalent admittance is given by equation (14). The equivalent circuit of the proposed

3rd order Combline bandpass filter is given in Figure 5.

$$Y_r = \frac{Y_0}{\tan\theta} \tag{14}$$

The resonator admittances and coupling admittances values are calculated from the equation given in (15) - (18). where the constant parameter n_r is the admittance constant [43].

$$Y_{r,r+1} = \left[\frac{K_{r,r+1}\tan(\theta_0)}{n_r n_{r+1}}\right]; \qquad r = 1, 2, \ldots N\text{-}1 \tag{15}$$

The scaled impedances to 50 Ω of the resonators Z_r and the coupling impedances $Z_{r,\,r+1}$ between adjacent resonators is calculated directly from the admittances as given by equations (16) and (18). The equivalent circuit of the proposed 3rd order Combline bandpass filter is given in Figure 6.

$$Z_r = Z_o * \left(\frac{1}{Y_r}\right) \tag{16}$$

$$Z_{r,r+1} = Z_o * \left(\frac{1}{Y_{r,r+1}}\right) \tag{17}$$

$$C_n = \frac{C}{Z_o} \tag{18}$$

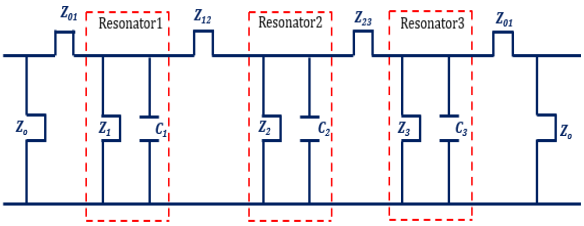

Figure 6: Equivalent circuit of the proposed 3rd order Combline bandpass filter with scaled impedance values.

F. Determination of Resonators Admittances

The physical dimensions of the bandpass filter are the length L, width W and thickness t of the resonators as well as the spacing or gap (G) between the resonators. However, for the Combline bandpass filter structure, the length of the resonator is the most important physical parameter as it is related to the passband centre frequency. The guided wavelength is given by (19) [43].

$$\lambda_g = \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}} = \frac{c}{f\sqrt{\varepsilon_{eff}}} \tag{19}$$

where λ_0 is the free space wavelength at the operating frequency and c is the speed of light (3.0 x 10^8 m/s) in free space. The propagation constant β and phase velocity v_p are given by (20)

$$\beta = \frac{2\pi}{\lambda_g} \quad ; \quad v_p = \frac{\omega}{\beta} = \frac{c}{\sqrt{\varepsilon_{eff}}} \tag{20}$$

The expression relating the physical length L of the resonator to the electrical length θ_o is given by (21) [46].

$$\theta_o = \beta L \tag{21}$$

Therefore, the physical length is given by (22) [43, 46].

$$L = \left(\frac{\theta_o}{2\pi f}\right)\left(\frac{c}{\sqrt{\varepsilon_{eff}}}\right) \tag{22}$$

For a tapped Combline bandpass filter, the tapped line is always taken to be of 50 Ω, and it is tapped points are located at a length of ϕ from the short-circuited end of the resonator to the ground and it is given by (23) [47].

$$\phi = \frac{\sin^{-1}\left(\sqrt{Y(\sin\theta)^2 / Y_o g_0 g_1}\right)}{1 - FBW/2} \tag{23}$$

Practical filters contain components with inherent finite resistance which affects the performance of the filter and are used to measure the quality of the filter. The effect of this resistance is related to the Quality factor or Q-factor. Q-factor is a measure of the loss in a filter which could be due to dielectric, conduction, and radiation. The quality factor is usually specified as unloaded-Q (Q_u) and external-Q (Q_e). For an N^{th} order filter, the Q_u is given by (24) [43].

$$Q_u = \frac{4.343 f_o}{(BW)L}\sum_{i-1}^{N} CL_i \tag{24}$$

The Combline bandpass filter external quality factors and coupling coefficients parameters are given by (25), (26) and (27) [1, 44].

$$Q_{e1} = \frac{g_0 g_1}{FBW} \tag{25}$$

$$Q_{en} = \frac{g_N g_{N+1}}{FBW} \tag{26}$$

© OCT 2025 | IRE Journals | Volume 9 Issue 4 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I4-1711457-8358

$$M_{i,i+1} = \frac{FBW}{\sqrt{g_i g_{i+1}}} \qquad \text{for } i = 1 \text{ to } N\text{-}1 \qquad (27)$$

G. Parameter Extraction for Coplanar

Effective dielectric constant ε_{eff} and characteristic impedance Z_o are very important design parameters of a coplanar waveguide with a known dielectric substrate. The expressions to determine ε_{eff} and Z_o are analytically derived based on conformal mapping techniques [48-50]. The ε_{eff} takes into consideration the geometry of a transmission line and it is always less than the dielectric constant ε_r. Figure 7 illustrates the cross-sectional view of Combline implemented in CPW structure.

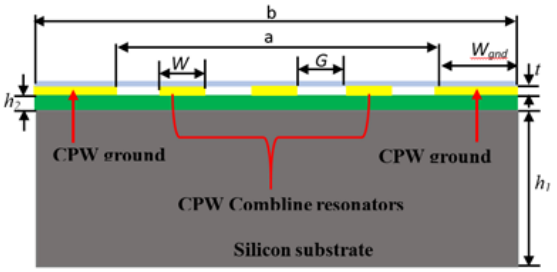

Figure 7: Cross-sectional view of the Combline CPW

The figure shows the parameters of the coplanar waveguide structure with resonator width W, $G_{k, k+1}$ is the gap between resonator k and $k+1$, a ground-to-ground inner spacing of 'a', ground-to-ground outer spacing of 'b', silicon substrate thickness (h_1) with relative permittivity $\varepsilon_{r1} = 11.9$, silicon dioxide thickness (h_2) with relative permittivity $\varepsilon_{r2} = 4.0$, conductor thickness (t) and W_{gnd} as the width of the ground plane. The resonator width can be utilised to limit the conductor loss and the spacing between the resonator and ground plane determines the characteristic impedance, Z_o. The total capacitances C_{cpw} of the *CPW* structure is the summation of the partial capacitances C_1, C_2 and C_{air} in the partial regions as given by (28) [48].

$$C_{cpw} = C_1 + C_2 + C_{air} \qquad (28)$$

where C_1 and C_2 represent the partial capacitances of the CPW within the two dielectric layers present. C_{air} represent the partial capacitance with the absence of all the dielectric layers. The effective permittivity and characteristic impedance of the structure are given by (29) and (30) [48].

$$\varepsilon_{eff} = \frac{C_{CPW}}{C_{air}} \qquad (29)$$

$$Z_0 = \frac{1}{cC_{air}\sqrt{\varepsilon_{eff}}} \qquad (30)$$

where c is the velocity of light in free space. For a coplanar waveguide structure with a very thick substrate and no ground on the backside and with perfect conductors, the effective dielectric constant is approximately equal to the average of the dielectric constant of the substrate as given by (31) [46].

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} \qquad (31)$$

III. IMPLEMENTATION OF THE BANDPASS FILTER

After the synthesis of the bandpass filter using the appropriate equations, the filter equivalent circuit was simulated in Keysight ADS software to predict the filter response. Electromagnetic field simulator software is used to design the 3D model. The computer simulation technique (CST) microwave studio was used to simulate the large-scale prototype and the High-Frequency Structural Simulator (HFSS) was used to simulate the proposed miniaturised CMOS compatible bandpass filter.

A. Equivalent Circuit Model Implementation

Table 2 shows the calculated resonator impedances to ground Z_r, coupling impedance values between the Combline resonators $Z_{r, r+1}$ and the capacitance "C" value, respectively.

Table 2: Resonator Impedances and Coupling Impedances

Symbol	Values	Unit
Z_0	117.4586	Ω
Z_1	119.2874	Ω
Z_2	69.9905	Ω
Z_3	119.2874	Ω
Z_4	117.4586	Ω
Z_{01}	87.0598	Ω
Z_{12}	350.1183	Ω
Z_{23}	350.1183	Ω
Z_{34}	87.0598	Ω
C	4.4516×10^{-14}	F

© OCT 2025 | IRE Journals | Volume 9 Issue 4 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I4-1711457-8358

Figure 8 shows the Chebyshev Combline bandpass filter designed and simulated in ADS using transmission lines sections of electrical length 50°.

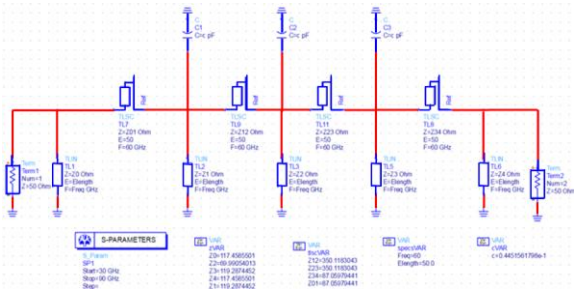

Figure 8: ADS Equivalent model of the bandpass filter.

The generated s-parameter response of the Chebyshev bandpass filter is based on the modelling parameters using the MAPLE software tool and the ADS equivalent schematic implementation as shown in Figure 9 and Figure 10.

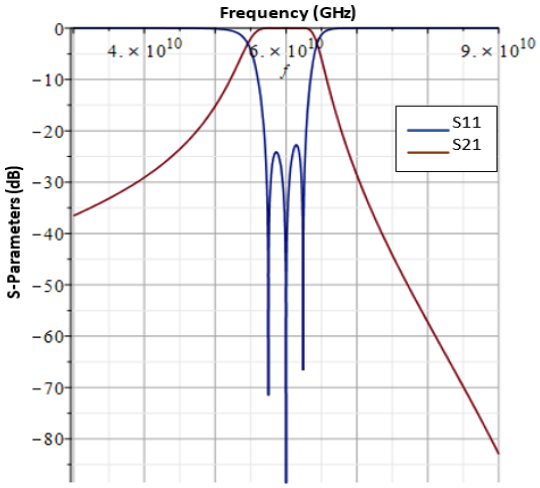

Figure 9: MAPLE S-Parameter response

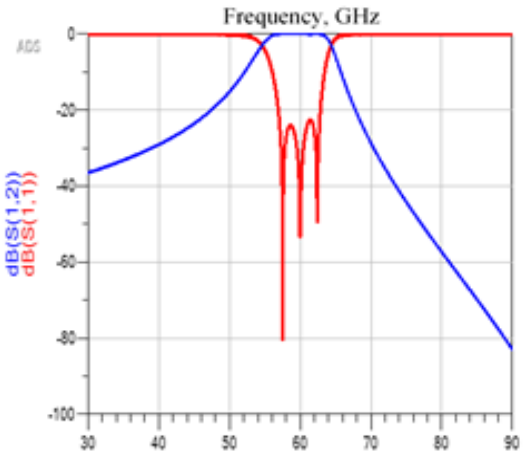

Figure 10: ADS S-parameters response

IV. THE CMOS 3D MODEL LAYOUT DESIGN

The 3D model layout of the bandpass filter was designed using the High Frequency Structure Simulator (HFSS), a finite element electromagnetic simulator from ANSYS. Figure 3.20 shows the complete process flow of ANSYS HFSS layout and simulation implemented in the filter design.

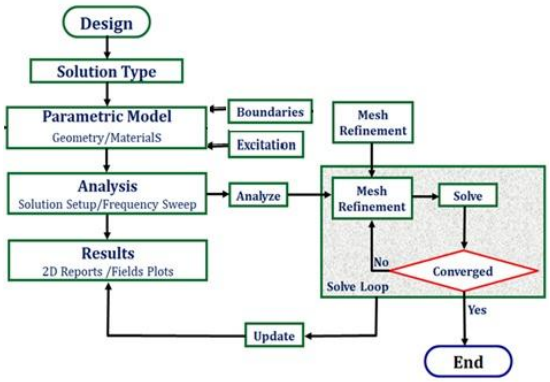

Figure 11: Process flow of ANSYS HFSS 3D Layout

The CMOS 3D layout of the coplanar waveguide model is the 3D model which is the proposed bandpass filter in terms of the physical design and the properties of the materials compatible with the CMOS process technology as show in Figure 12 and Figure 13.

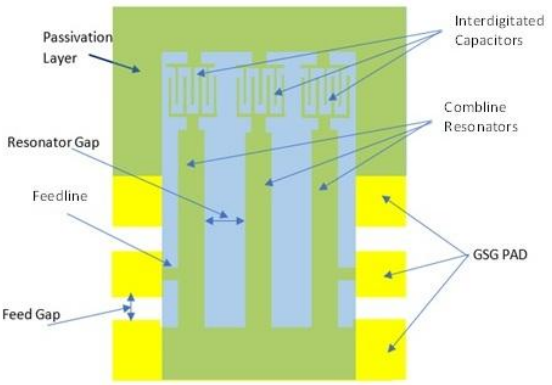

Figure 12: Schematic design of the top view

The CMOS process requires four layers of material design compatibility which are: the silicon (Si) substrate of the relative permittivity of 11.9, silicon dioxide (SiO_2) of relative permittivity 4.0, Aluminum (Al) conductor of the relative permittivity of 1.0 and lastly, the passivation layer is made of Silicon Nitride (Si_3N_4) of the relative permittivity of 7.0. Also, the G-S-G pads are introduced for RF input/output.

© OCT 2025 | IRE Journals | Volume 9 Issue 4 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I4-1711457-8358

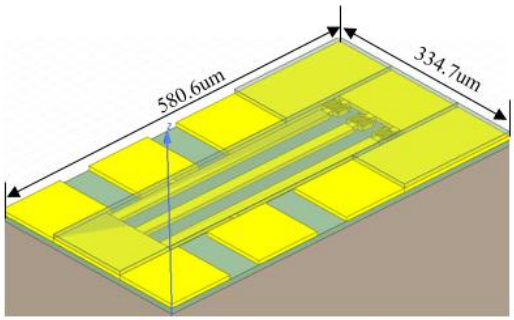

Figure 13: The 3D CMOS CPW bandpass filter

Table 3 and Table 4 show the values of the various physical dimensions of the proposed CMOS compatible filter and the interdigitated capacitor.

Table 3: Dimension of the CMOS CPW IDC

Symbol	Parameter	Values
N	Number of fingers	7 µm
W_f	Finger width	2.7 µm
S_f	Fingers Spacing	1.8 µm
L_f	Length of fingers	15 µm
W_T	Terminal strip width	2.2 µm
W_{FI}	Input line width	10.7 µm
L_{FI}	Input line length	8.6 µm
G_{ef}	Finger end of Gap	2 µm
L_c	Capacitor length	36.4 µm
W_c	Capacitor width	29.7 µm

Table 4: Physical Dimensions of the CMOS Filter

Symbol	Parameters	Values
H	Substrate Height	710 µm
t_r	Resonator thickness	0.975 µm
L_r	Resonator length	362.0 µm
W_r	Resonator width	17.9 µm
G_r	Resonator Gap	30.0 µm
Si_3N_4	Passivation thickness	1.75 µm
SiO_2	Silicon Dioxide	40 µm
L_P	Pad length	1.0 µm
W_p	Pad width	100 µm
G_f	Feed gap	100 µm
W_F	Feed Line Width	7.0 µm
L_F	Feed Line length	10.5 µm
W_G	Ground width	100 µm
ϕ	Tapped point	90 µm

Figure 14 shows the filter achieves a passband insertion loss performance of 0.03 dB and return loss performance better than 29.4 dB in the passband. The lower edge rejection is better than 60 dB at DC and upper edge rejection of 33.6 dB and transmission zero at 76.6 GHz. The equal ripple bandwidth is 9.8 GHz within a frequency range of 57.9 - 67.7 GHz with a fractional bandwidth of 16.3%

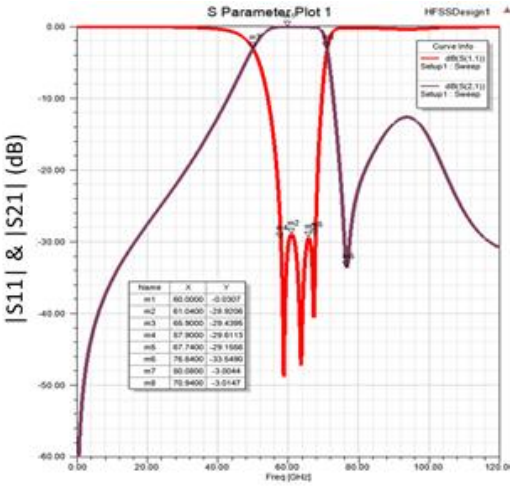

Figure 14: HFSS Simulation s-parameter response.

A. CMOS 0.18µm Design Rules Implementation

CMOS technology has many design rules that must be satisfied. These rules depend on the chosen process technology. They are the three most important rules that apply to all the processes for designing any passive components. The three rules are stated as follows: 1) Maximum Metal Track Rule or "Wide Rule" requires the use of metal slots for any metal width that exceeds 35 µm. 2) Minimum Metal Density Rule: The minimum metal density of 30% for the total fabricated area or metal dummies should be periodically inserted. 3) Minimum Metal Layer Rule: Requires device to be fabricated to occupy a minimum of three metal layers with each metal layer separated by silicon dioxide as an insulator. These three rules must be satisfied for the device to be fabricated to pass the design rule test. To meet these rules, the proposed miniaturised Chebyshev coplanar waveguide Combline bandpass filter model presented in Figure 13 is modified to the model shown in Figure 15.

© OCT 2025 | IRE Journals | Volume 9 Issue 4 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I4-1711457-8358

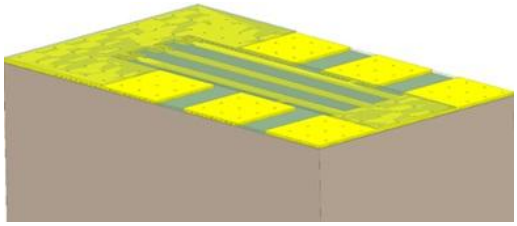

Figure 16: CMOS design rules consideration model

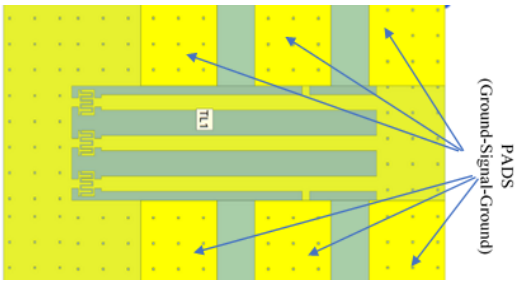

Figure 17: Top view of the CMOS model with metal slots

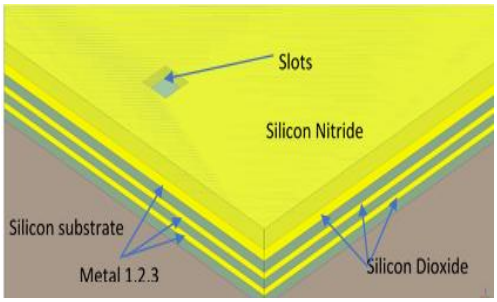

Figure 18: Sectional view showing metals and oxides layers.

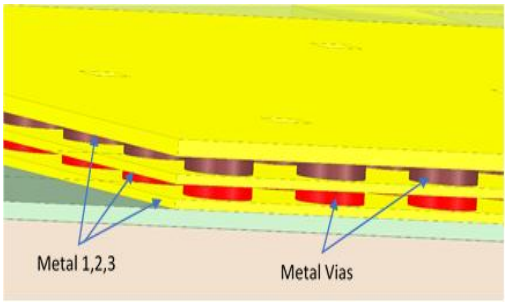

Figure 19: The 3D model showing vias interconnect.

Figure 20 shows the E-field intensity distribution of the bandpass filter at the centre frequency of 60 GHz. The red colour area indicates the high current density areas with strong coupling electric field while the bright colours (Blue, Green and yellow) area indicates low current density with low or weak coupling electric field. The simulated conductors are perfect conductor; therefore, all electrons are at the conductor surface. There is no electric field inside the conductor. The operating frequency of 60 GHz is in the passband; there are strong RF fields coupled between resonators.

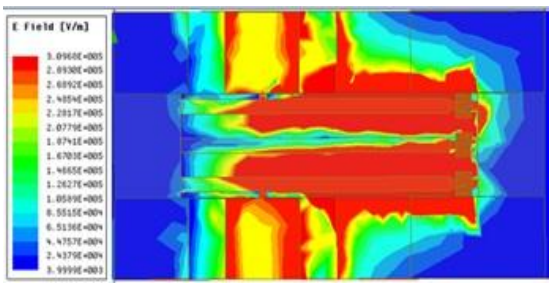

Figure 20: Current density/E-field intensity distribution across the Bandpass Filter

Figure 21 shows the mesh overlay of the bandpass filter.

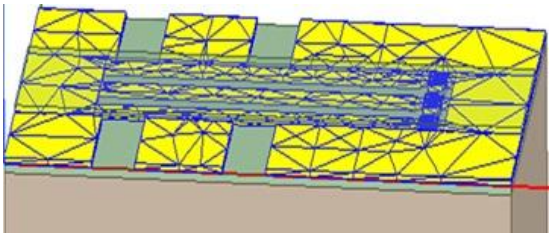

Figure 21: HFSS Mesh overlay plot of the bandpass filter

Figure 22 shows the s-parameter response of the 3D miniaturised CMOS compatible coplanar waveguide Combline bandpass filter with the design rules implemented. The response shows a slightly degraded performance with the consideration of the CMOS design rules in terms of the the shift the center frequency, insertion loss (S_{11}) and return loss (S_{21}) performance when compared to the response without the design rules considerations of Figure 12. This degraded performance can be attributed to the two dummy metal layers (MET1 and MET2) and metal slots inserted periodically in the structure to satisfy the design rules. This can also be attributed to the vias used to create a thick metal around the ground plane for linearity.

© OCT 2025 | IRE Journals | Volume 9 Issue 4 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I4-1711457-8358

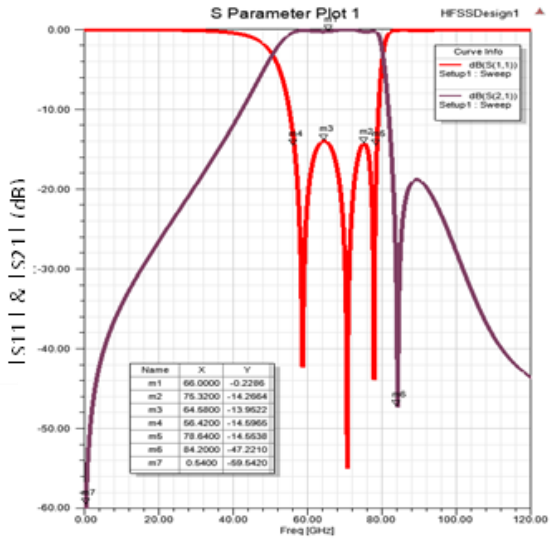

Figure 22: S-parameter response at 66GHz.

An insertion loss (IL) of 0.22 dB and return loss (RL) of 14.26 dB is achieved when compared to the insertion loss of 0.03 dB and return loss of 29.4 dB. However, a better stopband attenuation (SBA) of 47.2 dB is achieved at 84.2 GHz when compared to stopband attenuation of 33.5 dB achieved at 76.6 GHz when compared to the model without design consideration. To provide resonance at a centre frequency of 60 GHz, the resonator length is tuned to 401µm. The filter total size measures 619.6 µm by 334.7 µm while the core size measure 439.6 µm by 127.7 µm. The S-parameter response is shown in Figure 23.

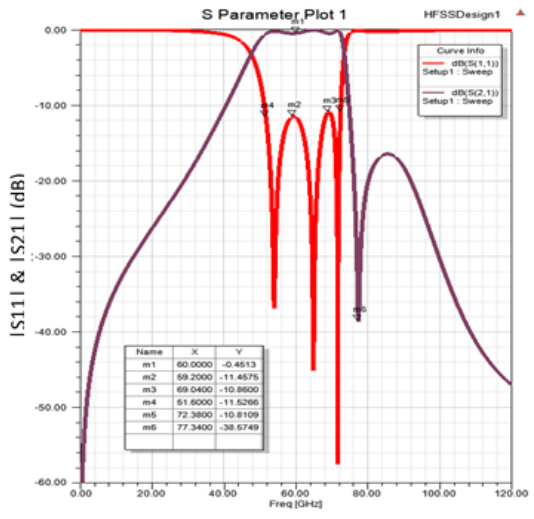

Figure 23: S-parameter response at 60GHz

IV DESIGN RULE CHECK AND PHYSICAL VERIFICATION PROCESS.

The simulated 3D model is then tapped-out in GDSII file format for design rules verification, physical violation checks using the XFAB XC0.18 µm CMOS process technology which can be fabricated in the foundry. Figure 24 shows the GDSII MET1-MET2-METTP metal layout of the 3D model. The result of the design rule and physical verification check is given in Table 6.

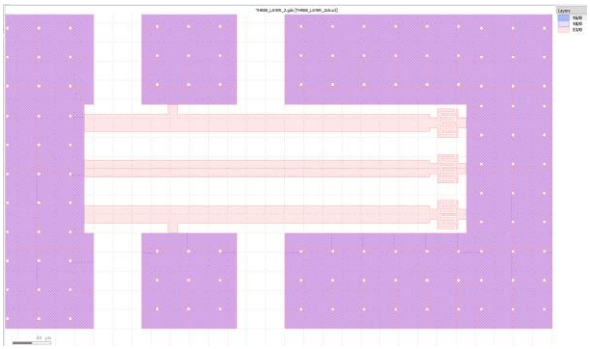

Figure 24: GDSII three layers layout of the 3D model.

As shown in the result, the design rule violation check was done for four models (SINGLE_LAYER_16, SINGLE_LAYER_33, THREE_LAYER_1 AND THREE_LAYER_2) of the miniaturised CMOS coplanar waveguide bandpass filter in the XFAB Foundry, Sdn, BhD using the XC0.18 µm and XP0.18 µm CMOS process technology.

Table 6: Design rule check and physical verification results

Cadence tool version - Cadence virtuoso IC6.1.8.100 - Cadence pvs19.12 XFAB technology PDK and DRC version: - XC018 Cadence pdk v3.4.2 - XC018 Cadence pvs v3.4.3 Result from DRC run: SINGLE_LAYER_16: - B1M1 SINGLE_LAYER_33: - B1MT THREE_LAYERS_1: - THREE_LAYERS_2: - B1M1 - B1M2 - B1MT - W1MT	Cadence tool version - Cadence virtuoso IC6.1.8.100 - Cadence pvs19.12 XFAB technology PDK and DRC version: - XP018 Cadence PDK v6.1.2 - XP018 Cadence pvs v6.1.2.1 Result from DRC run: SINGLE_LAYER_16, the following 2 rules are violated - B1M1 - R2M1 – 78.87% SINGLE_LAYER_33, the following 2 rules are violated - B1MT - R2MT – 80.11% THREE_LAYERS_1, the following 3 rules are violated - R2M1 – 73.45% - R2M2 – 73.45% - R2MT – 80.65% THREE_LAYERS_2, the following 7 rules are violated - R2M1 – 73.54% - R2M2 – 73.54% - R2MT – 80.71% - B1M1 - B1M2 - B1MT - W1MT

© OCT 2025 | IRE Journals | Volume 9 Issue 4 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV9I4-1711457-8358

From the results obtained, the four models have no design rules violations based on the XC0.18 µm CMOS process technology. Therefore, it means the four models passed the design rules and physical verification checks. Therefore, are compatible with the XC0.18 µm process technology. When designing using the CMOS technology design rules, violations can be rectified in the model or waived based on the severity and provided there are no fatal violations. Table 7 Shows performance comparison of CMOS bandpass filters from the literature.

Table 7: Performance Comparison of CMOS Bandpass Filters from the Literature with the Proposed Filter.

Ref.	CMOS (µm)	3 dB Freq, (GHz)	Size (mm^2)	IL (dB)	RL (dB)	Lower SBA (dB)	Upper SBA (dB)
[21]	0.18	-	0.12	5	10	55	50
[22]	0.18	48–72	0.16	5	15	27	38
[27]	0.18	50–80	1.71	4.9	10	32	55
[28]	0.13	57–66	0.21	1.5	9.2	45	35
[29]	0.18	50–70	0.59	2.77	27.5	23	6
[30]	0.18	63– 88	0.07	3	20	60	45
[31]	0.18	53–72	0.09	2.85	18	29	37
[32]	0.18	45–68	0.07	3.2	31	50	22
[38]	0.18	75–84	0.08	3.9	20	26	38
This work	0.18	50–70 50–70	0.19 0.19	0.03 0.22	29.4 14.0	>60 >60	33.7 47.2

V. CONCLUSION

In this paper, a miniaturised CMOS compatible coplanar waveguide Combline bandpass filter for 60 GHz millimetre wave for 5G application is presented. The simulated result for the miniaturised CMOS single metal layer bandpass filter shows an insertion loss of 0.03 dB, return loss better than 29 dB and a core chip size of 400.6 µm x 127.7 µm. Three metal layers model with CMOS design rules consideration shows an insertion loss of 0.45 dB and return loss better than 10.8 dB with a core size of 439.6 µm x 127.7 µm at 60 GHz millimetre-wave frequency band. The models show comparable or better performance with those reported in the literature which means the proposed Coplanar waveguide bandpass filter is a good candidate for millimetre-wave 5G application.

APPENDIX

A. CMOS XC0.18µm Layout and Design Rules Consideration

The design rules are a set of layer-by-layer process control structural and geometrical parameters or rules that must be satisfied to enable the device to pass the technology design rules checks and physical verification test such as metal width, spacing and thickness specifications.

Table 3.6: CMOS 0.18 µm Technology Width Design Rules

Rule	Description	Value	unit
W1MT	Minimum METTP width	0.44	µm
S1MT	Minimum METTP spacing / notch	0.46	µm
S2MT	Minimum METTP spacing to WIDE_METTP	0.60	µm
A1MT	Minimum METTP area	0.562	$µm^2$
R1MT	Minimum ratio of METTP area to die area	30	%
R1MTP1	The maximum ratio of METTP area to connected GATE area	400	µm
R2MTP1	The maximum ratio of METTP area to connected GATE area	400	µm
W4MT	Minimum METTP width joining wide METTP track (> 35 µm)	10.0	µm
S4MT	Minimum METTP spacing / notch for different net	0.80	µm

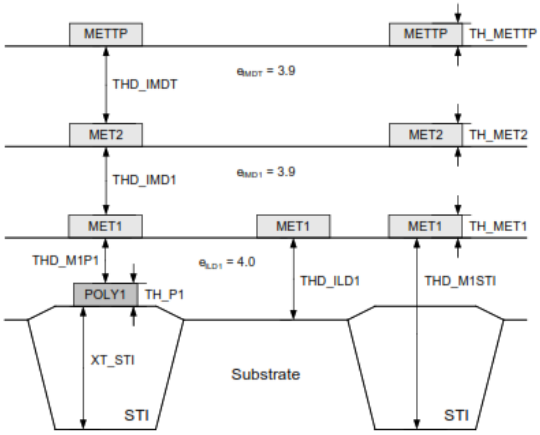

Figure 25: Standard metal layers of XC0.18µm CMOS technology

Table 3.7: Process control (Structural and geometrical) parameters

Parameter	Symbol	Min	Typ	Max	Unit
Metal 1 thickness	TH_MET1	495	555	615	nm
Metal 2 thickness	TH_MET2	495	555	615	nm
Top metal thickness	TH_METTP	875	975	1075	nm
Metal 1 – field dielectric thickness	THD_M1STI	1240	1390	1540	nm
Metal 1 – active dielectric thickness	THD_ILD1	840	990	1140	nm
Metal 1 – poly 1 dielectric thickness	THD_M1P1	640	790	940	nm
Metal 2 – metal 1 dielectric thickness	THD_IMD1	750	850	950	nm
Top metal – metal 2 dielectric thickness	THD_IMDT	890	1000	1110	nm
Passivation thickness	THV	1570	1750	1930	nm
Bulk wafer: wafer substrate resistivity	RSPWAF	8	10	12	Ω.cm
Wafer thickness	TH_WAF	710	725	740	µm

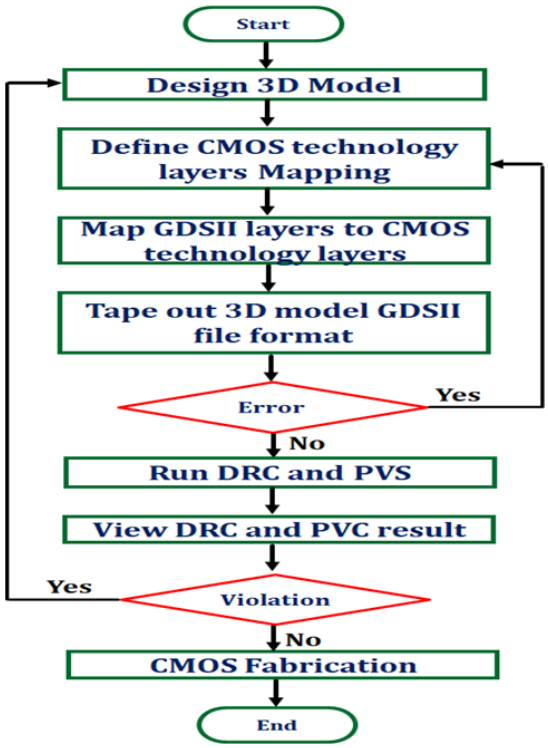

Figure 26: Design rule check and physical verification process.

ACKNOWLEDGMENT

The authors acknowledge Universiti Teknologi PETRONAS and Edo State University Iyamho for providing the research facilities and support for this research.

REFERENCES

[1] A. B. E. Elsaidy, A. B. Abdel-Rahman, A. Allam and R. K. Pokharel, "Ultra-compact CMOS 60-GHz Tapped-Line Combline BPF With Two Transmission Zeros Using Defected Ground Structures," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. vol. 8, no. no. 9, pp. pp. 1642-1649, 2018.

[2] "Implementing High Performance Filters in Millimeter Wave Applications," *Knowles Precision Devices Whitepaper,* vol. WP18TF02, pp. 1-5, April 2018.

[3] M. T. G. a. T. O. C. Seker, "A Review of Millimeter Wave Communication for 5G," *2nd International Symposium on Multidisciplinary Studies and Innovative Technologies (ISMSIT), Ankara,* pp. 1-5, 2018, doi: 10.1109/ISMSIT.2018.8567053.

[4] K. P. Devices, "Implementing High Herformance Filters in Millimeter-wave Applications," *whitepaper,* 2018.

[5] Y. I. Al-Yasir, N. Ojaroudi Parchin, R. A. Abd-Alhameed, A. M. Abdulkhaleq, and J. M. Noras, "Recent progress in the design of 4G/5G reconfigurable filters," *Electronics,* vol. 8, no. 1, p. 114, 2019.

[6] Y. Al-Yasir, R. A. Abd-Alhameed, J. M. Noras, A. M. Abdulkhaleq, and N. O. Parchin, "Design of very compact combline band-pass filter for 5G applications," 2018.

[7] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE Journal of Solid-State Circuits,* vol. 40, no. 1, pp. 144-155, 2005, doi: 10.1109/jssc.2004.837251.

[8] J. Laskar, S. Pinel, D. Dawn, S. Sarkar, B. Perumana, and P. Sen, "The next wireless wave is a millimeter wave," *Microwave Journal,* vol. 50, no. 8, p. 22, 2007.

[9] T. S. Rappaport *et al.*, "Wireless communications and applications above 100 GHz: Opportunities and challenges for 6G and beyond," *IEEE Access,* vol. 7, pp. 78729-78757, 2019.

[10] A. Vosoogh, A. A. Brazalez, and P.-S. Kildal, "A V-Band Inverted Microstrip Gap Waveguide End-Coupled Bandpass Filter," *IEEE Microwave and Wireless Components Letters,* vol. 26, no. 4, pp. 261-263, 2016, doi: 10.1109/lmwc.2016.2538598.

[11] L. Jong-Hoon, S. Pinel, J. Papapolymerou, J. Laskar, and M. M. Tentzeris, "Low-loss LTCC cavity filters using system-on-package technology at 60 GHz," *IEEE Transactions on Microwave Theory and Techniques,* vol. 53, no. 12, pp. 3817-3824, 2005, doi: 10.1109/tmtt.2005.859864.

[12] D. Wang, Y. Wu, K.-S. Chin, W. Che, and C.-C. Chang, "Compact 60 GHz low-temperature cofired ceramic filter with quasi-elliptic bandpass response," *IET Microwaves, Antennas & Propagation,* vol. 10, no. 6, pp. 664-669, 2016, doi: 10.1049/iet-map.2015.0694.

[13] J. K. Seonho Seok, and Nathalie Rolland "Wideband 60 GHz bandpass filter based on flexible PerMX polymer substrate," *IEEE,* 2012.

[14] T. S. Rappaport, J. N. Murdock, and F. Gutierrez, "State of the art in 60-GHz

integrated circuits and systems for wireless communications," *Proceedings of the IEEE,* vol. 99, no. 8, pp. 1390-1436, 2011.

[15] S. XU, F. MENG, K. MA, and K. S. YEO, "State of the Art in Passive Bandpass Filter Solutions for 60 GHz Communications GHz Communications," *ZTE COMMUNICATIONS,* vol. 14, no. S1, p. 1, 2016.

[16] H.-R. Chuang, L.-K. Yeh, P.-C. Kuo, K.-H. Tsai, and H.-L. Yue, "A 60-GHz Millimeter-Wave CMOS Integrated On-Chip Antenna and Bandpass Filter," *IEEE Transactions on Electron Devices,* vol. 58, no. 7, pp. 1837-1845, 2011, doi: 10.1109/ted.2011.2138141.

[17] S.-C. Chang *et al.*, "Compact Millimeter-Wave CMOS Bandpass Filters Using Grounded Pedestal Stepped-Impedance Technique," *IEEE Transactions on Microwave Theory and Techniques,* 2010, doi: DOI: 10.1109/TMTT.2010.2086591.

[18] A.-L. Franc, E. Pistono, D. Gloria, and P. Ferrari, "High-Performance Shielded Coplanar Waveguides for the Design of CMOS 60-GHz Bandpass Filters," *IEEE Transactions on Electron Devices,* vol. 59, no. 5, pp. 1219-1226, 2012, doi: 10.1109/ted.2012.2186301.

[19] N. Lan, K. Mouthaan, X. Yong-Zhong, S. Jinglin, S. C. Rustagi, and O. Ban-Leong, "Design of 60- and 77-GHz Narrow-Bandpass Filters in CMOS Technology," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 55, no. 8, pp. 738-742, 2008, doi: 10.1109/tcsii.2008.922427.

[20] S. Sun, J. Shi, L. Zhu, S. C. Rustagi, and K. Mouthaan, "Millimeter-Wave Bandpass Filters by Standard 0.18μm CMOS Technology," *IEEE Electron Device Letters,* vol. 28, no. 3, pp. 220-222, 2007.

[21] L. K. Yeh, C. Y. Chen, and H. R. Chuang, "A Millimeter-Wave CPW CMOS On-Chip Bandpass Filter Using Conductor-Backed Resonators," *IEEE Electron Device Letters,* vol. 31, no. 5, pp. 399-401, 2010, doi: 10.1109/led.2010.2043333.

[22] K. Ma, S. Mou, and K. S. Yeo, "Miniaturized 60-GHz On-Chip Multimode Quasi-Elliptical Bandpass Filter," *IEEE Electron Device Letters,* vol. 34, no. 8, pp. 945-947, 2013, doi: 10.1109/led.2013.2265165.

[23] Y. Zhong, Y. Yang, X. Zhu, E. Dutkiewicz, K. M. Shum, and Q. Xue, "An On-Chip Bandpass Filter Using a Broadside-Coupled Meander Line Resonator With a Defected-Ground Structure," *IEEE Electron Device Letters,* vol. 38, no. 5, pp. 626-629, 2017, doi: 10.1109/led.2017.2690283.

[24] H. Shigematsu, T. Hirose, F. Brewer, and M. Rodwell, "Millimeter-wave CMOS circuit design," *IEEE Transactions on Microwave Theory and Techniques,* vol. 53, no. 2, pp. 472-477, 2005, doi: 10.1109/tmtt.2004.840758.

[25] H. Singh, R. Prasad, and B. Bonev, "The studies of millimeter waves at 60 GHz in outdoor environments for IMT applications: A state of art," *Wireless Personal Communications,* vol. 100, no. 2, pp. 463-474, 2018.

[26] Y. I. Al-Yasir, N. OjaroudiParchin, A. Abdulkhaleq, K. Hameed, M. Al-Sadoon, and R. Abd-Alhameed, "Design, simulation and implementation of very compact dual-band microstrip bandpass filter for 4G and 5G applications," in *2019 16th international conference on synthesis, modeling, analysis and simulation methods and applications to circuit design (SMACD)*, 2019: IEEE, pp. 41-44.

[27] C.-Y. C. Cheng-Ying Hsu, Huey-Ru Chuang, "A 60-GHz Millimeter-Wave Bandpass Filter Using 0.18-μm CMOS Technology," *IEEE Electron Devices Letters,* vol. Vol. 29, no. No. 3, 2008.

[28] B. Yang, E. Skafidas, and R. Evans, "Design of 60 GHz millimetre-wave bandpass filter on bulk CMOS," *IET microwaves, antennas & propagation,* vol. 3, no. 6, pp. 943-949, 2009.

[29] R. K. Pokharel, X. Liu, R. Dong, A. Dayang, H. Kanaya, and K. Yoshida, "60 GHz Millimeter-Wave CMOS Integrated On-Chip Open-Loop Resonator Bandpass Filter on Patterned Ground Shields," in *Institute of Electronics, Information and Communication Engineers (IEICE) TRANS. ELECTRON* 2013, vol. E96-C, no. 2, pp. 270-276.

[30] L.-K. Yeh, Y.-C. Chen, and H.-R. Chuang, "A novel ultra-compact and low-insertion-loss 77. GHz CMOS on-chip bandpass filter with adjustable transmission zeros," in *2014 44th European Microwave Conference*, 2014: IEEE, pp. 1056-1059.

[31] A. Barakat, R. Pokharel, and T. Kaho, "60 GHz on-chip mixed coupled BPF with H-shaped defected ground structures,"

Electronics Letters, vol. 52, no. 7, pp. 533-535, 2016, doi: 10.1049/el.2015.4465.

[32] E. Elsaidy, A. Barakat, A. B. Abdel-Rahman, A. Allam, and R. K. Pokharel, "Ultra-compact CMOS 60-GHz Tapped-Line Combline BPF With Two Transmission Zeros Using Defected Ground Structures," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. 8, no. 9, pp. 1642-1649, 2018, doi: 10.1109/tcpmt.2018.2861411.

[33] A. S. A. El-Hameed, A. Barakat, A. B. Abdel-Rahman, A. Allam, and R. K. Pokharel, "Ultra-compact 60-GHz CMOS BPF Employing Broadside-Coupled Open-Loop Resonators," *IEEE Microwave and Wireless Components Letters,* vol. 27, no. 9, pp. 818-820, 2017, doi: 10.1109/lmwc.2017.2734771.

[34] C.-Y. Hsu, et al., "A 70-GHz Millimeter-Wave Compact Bandpass Filter Fabricated Using Standard 0.18-μm CMOS Technology," *IEEE 38th European Microwave Conference.,* 2008.

[35] A. A. Saadi, M. C. E. Yagoub, A. Slimane, and R. Touhami, "Design of miniaturised CMOS bandpass filters for ultra-wideband applications," *AEU - International Journal of Electronics and Communications,* vol. 84, pp. 1-7, 2018, doi: 10.1016/j.aeue.2017.11.013.

[36] T. H. H. Shigematsu, F. Brewer and M. Rodwel, "Millimeter-wave CMOS circuit design," *IEEE Transactions on Microwave Theory and Techniques,* vol. vol. 53, no. no. 2, pp. pp. 472-477, 2005.

[37] X. Wang, Hsien-Shun Wu, and Ching-Kuang C. Tzuang. , "CMOS 170 GHz Combline Bandpass Filter," *IEEE MTT-S International Conference on Microwaves for Intelligent Mobility (ICMIM),* 2015.

[38] Y.-M. Chen and S.-F. Chang, "An ultra-compact 77-GHz CMOS bandpass filter using grounded pedestal stepped-impedance stubs," in *2011 41st European Microwave Conference*, 2011: IEEE, pp. 194-197.

[39] A. H. Reja, S. N. Ahmad, and M. A. Alqaisy, "Study the Effect of SRRs on Broadband Microwave parallel-coupled band-pass filters," *International Journal of Computer and Electrical Engineering,* vol. 6, no. 2, 2014.

[40] C. M. K. Richard J. Cameron, Raafat R. Mansour, "Microwave Filters for Communication Systems: Fundamentals, Design, and Applications," *John Wiley & Sons, Inc.,* 2018.

[41] S.-w. Wen, Y. Gao, D.-p. Zhang, and C. Han, "Modified design of microstrip interdigital filter with tapped line," in *Emerging Imaging and Sensing Technologies for Security and Defence III; and Unmanned Sensors, Systems, and Countermeasures*, 2018, vol. 10799: International Society for Optics and Photonics, p. 107990M.

[42] D. M. Pozar, "Microwave engineering," *Wiley,* 2012.

[43] I. Hunter, "Theory and design of microwave filters," *(United Kingdom: The Institution of Engineering & Technology),* 2001

[44] J.-S. G. Hong and M. J. Lancaster, *Microstrip Filters for RF and Microwave applications*. John Wiley & Sons, 2011.

[45] S. Tripathi, N. Pathak, and M. Parida, "Microwave front-end subsystems design for ITS/GPS applications," *Engineering Science and Technology, an International Journal,* vol. 19, no. 4, pp. 1815-1825, 2016.

[46] B. Pradhan and B. Gupta, "Ku-band RF MEMS tunable comb line band reject filter on coplanar transmission line," *AEU-International Journal of Electronics and Communications,* vol. 67, no. 6, pp. 463-469, 2013.

[47] V. G. Anupma Gupta, "Design of BPF Using Interdigital Bandpass Filter On Center Frequency 3GHz. ," *PhD Thesis,* 2015.

[48] R. N. Simons, *Coplanar waveguide circuits, components, and systems*. John Wiley & Sons, 2004.

[49] I. Wolff, *Coplanar microwave integrated circuits*. John Wiley & Sons, 2006.

[50] H. Shi, "Miniaturized planar RF integrated filters with good harmonic suppression," 2005.