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Analysis of Switching Frequency Effects on THD and Switching Losses in a Filtered Single-Phase SPWM Inverter

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Abstract- This paper investigates the effect of switching frequency on total harmonic distortion (THD) and switching losses in a single-phase sinusoidal pulse width modulation (SPWM) inverter with an LC output filter. Using MATLAB/Simulink, the inverter is modelled with a 400V DC input, H-bridge IGBTs and a damped LC filter designed to suppress high frequency harmonics. The switching frequency varied between 5KHz and 25KHz and output quality was evaluated through FFT analysis. The results show that THD remains extremely low (0.02-0.07%) across all tested frequencies due to the strong filtering effect of the LC, indicating that increasing switching frequency has no significant harmonic benefit. Conversely, switching losses varies linearly with frequency. The optimal operating frequency for the modelled system is 5KHz as it keeps the switching loss at the minimum while maintaining excellent waveform.

Index Terms- Switching Frequency, Total Harmonic Distortion (THD), Single-Phase Inverter, Switching Loss, Filter

I. INTRODUCTION

The demand for clean and efficient energy systems has driven the widespread adoption of renewable energy technologies such as solar and wind power [1]. Central to these systems are power electronic converters, particularly single-phase sine pulse width modulation (SPWM) inverters, which are valued for their simple structure, cost-effectiveness, and ability to produce near-sinusoidal output voltages [2]. These inverters are widely employed in grid-connected renewable systems, standalone power supplies, and power conditioning equipment. Despite their advantages, SPWM inverters inherently introduce current harmonics into the power system, which can degrade power quality, reduce overall performance, and potentially stress connected equipment [3]. One of the key design factors affecting both output voltage quality and efficiency in these systems is the switching frequency of the inverter.

One common way to improve inverter output quality is increasing the switching frequency because this method pushes the switching harmonics to higher frequencies thereby reducing low order distortion and improving the total harmonic distortion [4]. It is quite important to note that higher switching frequencies also increase switching losses, raise semiconductor thermal stress and may require more expensive components and thermal management [5] [10]. However, lower switching frequencies reduce switching losses and improve efficiency but often degrade waveform quality, since the output contains more low-frequency harmonic components. While this trade-off generally applies to unfiltered SPWM inverters, its behavior can differ significantly when an LC output filter is used. A strong LC filter can suppress most switching harmonics regardless of the switching frequency, meaning THD may not improve substantially even if the switching frequency is increased and yet switching losses will still rise [6] [9].

In filtered inverters, the LC network may dominate harmonic shaping, limiting the impact of switching frequency on output waveform quality [7]. Considering that increased switching frequency inherently enhances harmonic performance in both filtered and unfiltered SPWM inverters, yet concurrently elevates switching losses, the central design inquiry becomes: how should the switching frequency be optimally determined in filtered SPWM inverter architectures where the LC network predominantly governs harmonic attenuation?

This study investigates how switching frequency affects THD and switching losses in a single-phase SPWM inverter equipped with an LC output filter. MATLAB/Simulink simulations are used to evaluate inverter performance across different switching frequencies, with the aim of determining if increasing the switching frequency provides any meaningful harmonic benefit in a filtered inverter and identifying the most efficient switching frequency for the modeled system.

II. METHODOLOGY

2.1 System Overview

Figure 1 shows the circuit flowchart of a single-phase inverter, which consists of a DC source of 400 V, a full-bridge switching circuit (consisting of four insulated-gate bipolar transistors (IGBTs) with anti-parallel diodes) uses SPWM switching technology to convert DC 400 VDC to AC 110 or 220 V_{rms} with an LC filter. The driving signals of the full-bridge power switches are generated by the SPWM controller according to the SPWM control program and the inverter was operated with a modulation index of 0.81. The inverter was operated on an open loop mechanism as no close loop was implemented, hence the output voltage depends on the modulation index, DC voltage, filter characteristics and load impedance.

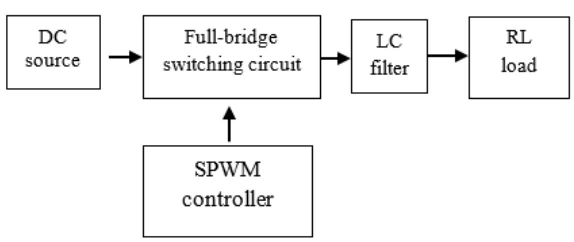

Figure 1: Single-phase full-bridge SPWM inverter circuit diagram showing H-bridge configuration with IGBTs, DC input, LC filter, and load

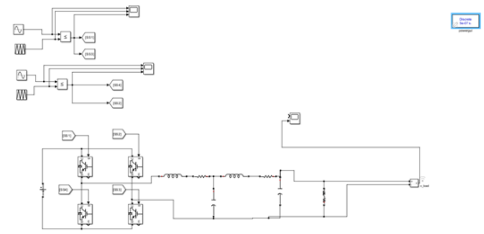

Figure 2:Modelled Single-phase full-bridge SPWM inverter circuit diagram showing H-bridge configuration with IGBTs, DC input, damped LC filter, and RL load on MATLAB

At the inverter output in figure 2, a damped LC filter was implemented to suppress high-frequency harmonics and recover a near-sinusoidal waveform. The filter parameters were selected to give a cutoff frequency slightly above the fundamental output frequency (50 Hz) but far below the switching frequency, thereby ensuring effective attenuation of switching harmonics. The output voltage, power delivered, and harmonic distortion were measured under each scenario using the MATLAB (Fast Fourier Transform) FFT analysis tool. The analysis was carried out on all the frequency simulated, the inverter supplied a fixed series RL load of 90Ω and 0.12H, representing a moderately inductive single-phase load. Under the nominal operating condition, the inverter delivered approximately 232 Vrms at 50 Hz across this load, corresponding to about 0.5 kW of real power with a power factor of around 0.9 lagging. This operating point was kept constant while the switching frequency was varied to study its effect on total harmonic distortion (THD) and switching losses.

2.2 Pulse Width Modulation

The inverter was controlled using the sinusoidal pulse width modulation (SPWM) technique. In this scheme, a sinusoidal reference signal is compared against a high-frequency triangular carrier waveform. The intersection points between the two signals determine the switching instants of the IGBTs in the H-bridge, thus generating a modulated output voltage waveform.

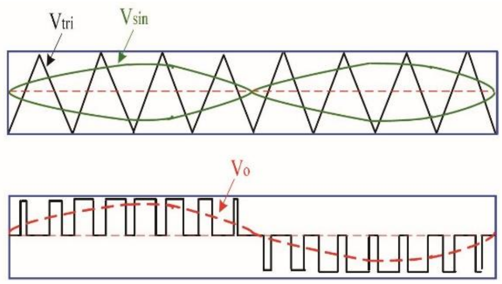

Figure 3: (Color online) SPWM generation showing sinusoidal reference and triangular carrier waveforms with intersection points indicating switching instants

The reference signal is expressed as:

$$V_{control}(t) = V_m \sin(\omega t) \qquad (1)$$

where V_m is the peak of the modulation signal and ω is the angular frequency of the fundamental output $(50\,Hz)$. The carrier signal is a high-frequency triangular waveform given by:

$$V_{carrier}(t) = V_c triangular\ (f_{sw} t) \qquad (2)$$

where V_c is the peak of the carrier and f_{sw} is the switching frequency.

The modulation index (M) is defined as:

$$M = \frac{V_m}{V_c} \qquad (3)$$

In this study, the modulation index was kept at 0.81 to ensure linear modulation and minimize waveform distortion. By varying the switching frequency (f_{sw}) between 5 kHz and 25 kHz in steps of 5 kHz, the impact of switching speed on harmonic distortion and output quality was systematically investigated.

2.3 LC Filter Design

To suppress switching-frequency harmonics and produce a clean sinusoidal output, a damped LC low-pass filter was connected at the inverter output. The cutoff frequency of the filter was selected to be slightly higher than the 50 Hz fundamental frequency but significantly lower than the switching frequency, ensuring that the fundamental component passes with minimal attenuation while higher-order harmonics are attenuated.

The cutoff frequency is given by:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \qquad (4)$$

In this study, the filter parameters were chosen as L = 20mH and C = 40μF, which resulted in a cutoff frequency of approximately 178 Hz. This design ensures that the 50 Hz fundamental passes unaffected, while switching harmonics in the kHz range are effectively suppressed. The resulting output voltage waveform is close to sinusoidal, suitable for AC load applications.

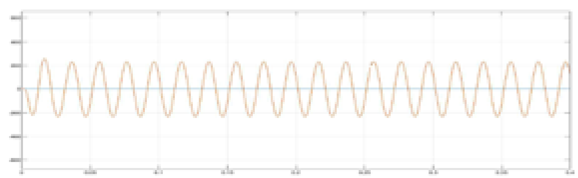

Figure 2: SPWM generation showing sinusoidal wave output of a 5KHz switching frequency.

2.4 Harmonic Distortion Analysis

The harmonic content of the inverter output voltage was quantified using Fourier analysis in MATLAB/Simulink. The PowerGUI FFT analysis tool was employed to evaluate the total harmonic distortion (THD) of the output waveform under each test condition. To ensure accuracy, transients were excluded by selecting a steady-state window of at least ten cycles of the fundamental frequency.
Total harmonic distortion is defined as:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100\% \qquad (5)$$

Where V_1 is the RMS value of the fundamental component of the output voltage, and V_n are the RMS values of the nth-order harmonics.

This metric provides a measure of waveform quality, with lower THD values indicating a waveform closer to the ideal sinusoidal reference. In line with IEEE Standard 519, a Maximum harmonic voltage distortion for systems rated 120 V through 69kV of less than 5% is typically required for acceptable power quality [8]. In this study, values of THD were recorded across all switching frequencies and load condition, allowing comparison of inverter performance under different operating scenarios.

2.5 Switching Loss Modeling

Inverter switching losses were estimated based on the overlap of device voltage and current during each transition. For each switching event, a finite rise and fall time occurs, during which the device simultaneously sustains voltage and conducts current, resulting in energy dissipation. The average switching power loss is approximated as:

$$P_{sw} \approx \frac{1}{2} V_{dc} I_{load} \left(t_{on} + t_{off}\right) f_{sw} \qquad (6)$$

where:

- V_{dc} is the input DC bus voltage,
- I_{load} is the load current,
- t_{on} and t_{off} are the device turn-on and turn-off transition times, and
- f_{sw} is the switching frequency.

From this relation, it is evident that switching losses increase linearly with frequency. In this study, typical IGBT switching times from manufacturer datasheets were assumed $(t_{on} = 200ns, t_{off} = 300ns)$. By applying this model across the tested load conditions, the relative increase in switching losses at different frequencies was quantified.

III. RESULTS AND DISCUSSION

3.1 For this study, the simulation was carried out using MATLAB/Simulink. The inverter model consists of four IGBT/diode switches, a DC source, an LC low-pass filter, current and voltage measurement blocks, an SPWM controller, and the PowerGUI analysis tool. The study investigates how different switching frequencies affect the performance of a single-phase SPWM inverter, focusing specifically on total harmonic distortion (THD) and switching losses. Although switching frequency is commonly varied to improve harmonic performance, the presence of a strong LC output filter may change this behaviour. FFT analysis is therefore used to evaluate THD at each switching frequency and determine whether increasing the switching frequency provides any additional benefit in the filtered inverter design.

3.2 Effect of Switching Frequency Effect on Output Quality

The simulation results for THD, output voltage, and power at different switching frequencies are presented in Figure 5 and Table 1.

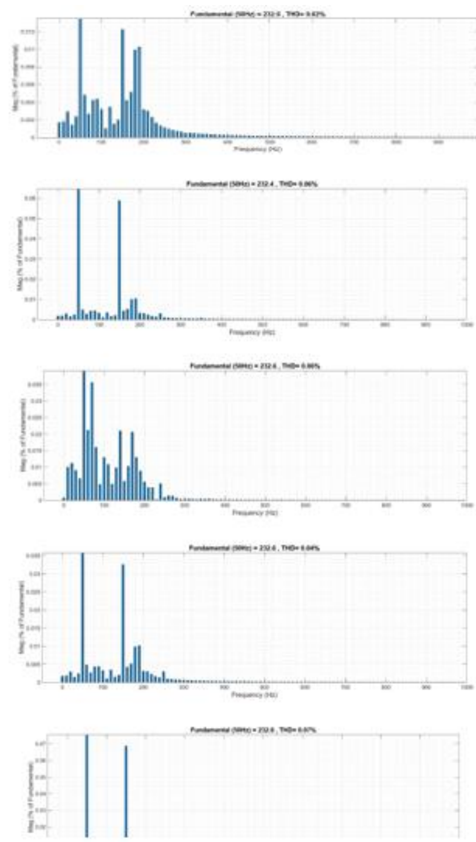

Figure 3: simulation results for THD and output voltage

Table 1: Effect of Switching Frequency on Output Quality

Switching frequency (kHz)	THD (%)	$V_{out}(V_{rms})$	Power(W)
5	0.02	232.6	511.2
10	0.06	232.4	509.8

15	0.06	232.6	511.2
20	0.04	232.6	511.2
25	0.07	232.8	512.9

The results show that THD remains extremely low (below 0.1%) across all tested switching frequencies, with the lowest value (0.02%) observed at 5 kHz. Interestingly, the THD does not show a consistent decreasing trend with increasing switching frequency as might be expected from theory. This could be attributed to the effective filtering provided by the LC filter design and the high modulation index used.

The output voltage remains stable at approximately 232.6 V across all switching frequencies, indicating good voltage regulation. Similarly, the power delivered to the load remains consistent at approximately 512 W, showing that the switching frequency does not significantly affect the power transfer capability of the inverter.

Table 2: Effect of Switching Frequency on switching losses

Switching frequency (KHz)	THD (%)	$V_{out}(V_{rms})$	**Switching Losses, f_{sw}(W)**
5	0.02	232.6	1.19
10	0.06	232.4	2.38
15	0.06	232.6	3.57
20	0.04	232.6	4.77
25	0.07	232.8	5.96

The results in Table 2 show that the switching losses increase almost linearly with switching frequency. The loss rises from 1.19 W at 5 kHz to 5.96 W at 25 kHz, which is roughly a five-fold increase for a five-fold increase in switching frequency. This behavior is consistent with the switching-loss model $P_{sw} \propto f_{sw}$,

where higher switching frequencies produce more voltage–current overlap transitions per second.

In contrast, the output-voltage THD remains extremely low (0.02–0.07%) for all frequencies due to the LC filter. Since THD does not significantly improve with higher switching frequency, the increasing switching losses become the dominant factor in selecting the operating point. Therefore, for this inverter configuration, 5 kHz is the most efficient switching frequency, providing the lowest switching loss while maintaining excellent waveform quality

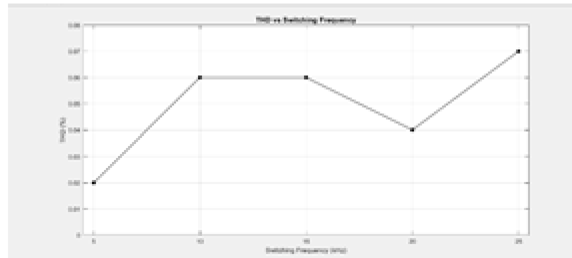

Figure 4: Graph showing THD vs. switching frequency

These findings suggest that for this inverter design with the specified filter parameters, the switching frequency can be selected based on other considerations (such as switching losses) without significantly compromising the output voltage quality.

3.3 Switching Loss Analysis

The switching losses were calculated using the model presented in Section 2.5. As expected, the switching losses increase linearly with switching frequency, as shown in Figure 6.

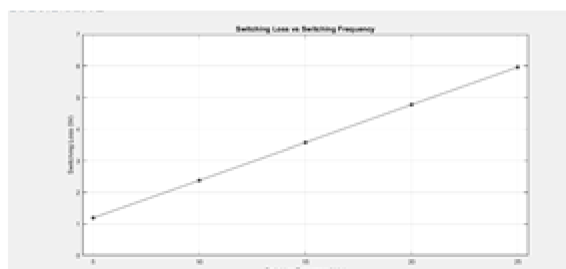

Figure 5: Graph of switching loss VS Switching Frequency

At 5 kHz, the switching losses are minimal, while at 25 kHz, they are approximately five times higher. This increase in switching losses directly impacts the overall efficiency of the inverter, particularly at higher frequencies

3.4 Discussion

The results of this study clearly show that switching frequency has two distinct effects on the simulated

SPWM inverter. First, the switching losses increase steadily with switching frequency, rising from 1.19 W at 5 kHz to 5.96 W at 25 kHz. This behavior is consistent with switching-loss theory, where higher switching frequencies introduce more voltage–current overlap transitions, resulting in greater energy dissipation per second.

In contrast, the output-voltage THD remains extremely low across all tested switching frequencies, varying only between 0.02% and 0.07%. This very small variation indicates that the LC output filter plays a dominant role in harmonic suppression. Since the filter already attenuates high-frequency components effectively, increasing the switching frequency does not significantly influence the harmonic content of the output voltage. This result differs from typical unfiltered or lightly filtered SPWM inverters, where increasing switching frequency directly improves THD by shifting harmonics to higher frequencies.

The comparison between switching losses and THD demonstrates that raising the switching frequency does not yield any harmonic-quality improvement for this inverter configuration, yet it increases switching losses substantially. As a result, efficiency becomes the determining factor in selecting an appropriate switching frequency. The lowest switching frequency tested, 5 kHz, provides the minimum switching losses while maintaining the same excellent harmonic performance as higher switching frequencies.

IV. CONCLUSION

This study presented an analysis of the relationship between switching frequency, total harmonic distortion, and switching losses in a single-phase SPWM inverter equipped with an LC output filter. The key findings are:

THD remains extremely low (0.02%–0.07%) for all tested switching frequencies, demonstrating that the LC output filter effectively dominates harmonic suppression in this inverter configuration.

Switching losses increase nearly linearly with switching frequency, highlighting the efficiency penalty associated with operating at higher switching frequencies.

Increasing the switching frequency does not provide any meaningful improvement in THD, since the LC filter already removes most of the switching harmonics.

The most optimal switching frequency for this design is 5 kHz, which yields the lowest switching losses while maintaining excellent waveform quality.

Overall, the results show that in filtered SPWM inverters, increasing the switching frequency offers no harmonic benefit and only increases switching losses. Therefore, for the modeled inverter parameters, a switching frequency of 5 kHz provides the best balance between power quality and efficiency. These conclusions apply specifically to the inverter configuration, load conditions, and filtering design used in this study.

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