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Memory Architectures for Robust IoT-Based Applications: A Comprehensive Study of 6T SRAM with Emphasis on Read-Write Operations, Stability, and Radiation Hardening

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Abstract- ***As the Internet of Things (IoT) ecosystem grows, so does the demand for efficient and dependable memory solutions targeted to the unique difficulties of IoT-based applications. The demand for reliable and energy-efficient Static random-access memory (SRAM) has risen due to the increasing number of Internet of Things (IoT) devices and the increase in semiconductor technology. Because of its simplicity, low standby power consumption, and ease of integration, the 6T SRAM cell is a good choice for Internet of Things applications. The 6-transistor (6T) SRAM cell has become popular because of its simplicity and adaptability. The study looks on the resistance of memory systems, namely the 6T SRAM cell, against radiation-induced errors. It is critical to understand how ionising radiation affects memory integrity in Internet of Things scenarios where devices may be exposed to radiation-rich environments. This paper presents a comprehensive study and simulation of the 6T SRAM cell for the use IoT applications, on cadence virtuoso tool with GPDK 45nm technology node focusing on its read-write operations, stability, and radiation-hardening properties.***

Keywords— IoT, SRAM, RSNM, Soft Error Rate, Radiation- Hardened

I. INTRODUCTION

The growing popularity of Internet of Things (IoT) technologies has brought about a new era of linked devices, demanding memory solutions that are not only efficient but also adaptable in changing and demanding environments. SRAM is a type of volatile memory that is primarily used to store and retrieve data quickly within electronic systems. It is often employed for tasks requiring high-speed access to data, such as caching and buffering in computer processors, graphics cards, and various embedded systems. SRAM is considered static because it doesn't require periodic refresh cycles like DRAM, making it faster in terms of data access. SRAM's primary role in modern semiconductor devices is to provide fast, low-latency data storage and retrieval capabilities. Its high-speed characteristics and stability make it well-suited for applications where rapid access to data is critical, enhancing the overall performance and responsiveness of electronic systems [1].

In the realm of space exploration, Static Random Access Memory, or SRAM, is used because of its stable performance, energy efficiency, and quick data access.

Engineers frequently use unique designs and methods to make it radiation-resistant, which is important considering the difficult conditions in space. This contributes to the success and endurance of space missions by ensuring that the memory not only functions effectively but also withstands the difficulties presented by the space environment [2].

Soft errors threaten the reliability of today's devices in the submicron region. An event caused by energetic particles has become a major reliability issue in advanced microelectronics [3]. Soft errors in SRAM refer to transient and correctable data errors caused by external factors, such as highly energetic charged particles. These particles are mainly made up of neutrons and alpha particles which form due to cosmic radiation and chip packaging. These particles strike directly or indirectly ionization in the silicon, affecting the signal charge at a circuit node and causing temporary malfunction. These types of errors are

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called soft errors because they do not always cause damage to the device permanently.

Typically, the critical charge Qcrit of SRAM is used to evaluate its soft error tolerance. In SRAM, critical charge Qcrit is defined as the is the least amount of the charge necessary to flip a data bit that contained in an SRAM cell. It has an inverse connection with the soft error rate (SER). The soft error rate (SER) grows exponentially as in Qcrit decreases linearly. Therefore, to limit SER, Qcrit needs to be as large as possible. However, the actual value of Qcrit in the SRAM chip data may differ from the design value due to the process effect caused by changes in the transistor's parameters. These include physical factors like channel length(L) and width (W), oxide thickness, and many more. Electrical parameters such as junction capacitance, threshold voltage (VTH), etc. The unpredictability rises as nanometre- scale technology improves, affecting the performance and production of nanometric SRAM [4]. In this paper section A discuss about the structure of SRAM and it's read write operation and section B discuss about stability and section C discuss about the Radiation-Hardened SRAM.

II. DESIGN METHODOLOGY

A. Working of 6T SRAM Cell

The term "6T SRAM" refers to a type of Static Random- Access Memory (SRAM) cell that is often used to store data in digital integrated circuits. The "6T" represents the number of transistors in the cell. The 6T SRAM cell is made up of six metal-oxide-semiconductor field-effect transistors (MOSFETs) that are organized in a certain way to achieve stability and dependability when storing binary data. The 6T SRAM cell is composed of two cross-coupled inverters, each of which includes a pair of complementary metal-oxide- semiconductor (CMOS) transistors. These inverters produce a bistable latch that can store a binary value (0 or 1). Additionally, it has two access transistors that can read and write states. Because of their bistable nature, the cross-coupled inverters keep the stored data as long as there is a power source. The SRAM cell is accessible when the word line (WL) is high. There is typically 6T SRAM cell in Figure 1.

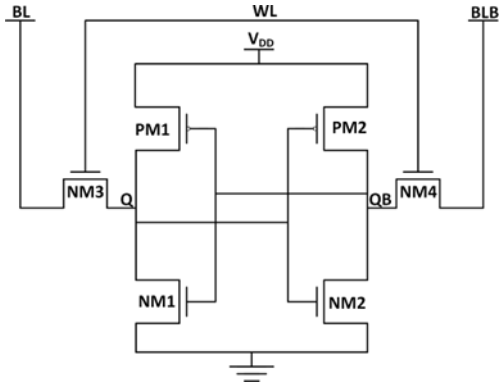

Figure1. 6T SRAM Cell

- Standby mode: When in standby mode, word line WL is 0, which turns off the two pass transistors NM3 and NM4, prevents access to the SRAM cell, and ensures that the contents of the coupled transistor stay unchanged as long as the supply voltage is present. A 6T SRAM cell's standby mode is a low-power state in which it is not actively involved in data access, but it saves the data it has stored and is prepared to switch to an active state at any time.
- Read mode: In read mode 6T SRAM cell is actively involved in retrieving stored data. The bitlines (BL and BLB) are precharged to a specified voltage level before to a read operation. This ensures that the read process has a well-defined beginning point. The wordline (WL) connected with the selected SRAM cell is turned on. This activates the access transistors NM3 and NM4, allowing the SRAM cell's storage nodes Q and QB to be connected to the bitlines. Firstly assume 1 is stored at the node, therefore the BLB will discharge through NM1 and the BL will be pulled up through PM1 to VDD. The transistors PM1 and NM2 are off in this mode of operation, whereas the transistors NM1 and PM2 are operating linearly. In Figure 2 it shows the discharging path during the read operation.

The voltage difference is amplified by the sense amplifiers, on the levels of voltage to determine which bit in the SRAM cell has been stored. A higher voltage on one bit line, for instance, might be associated with a recorded "1," and a higher voltage on the other bit line, with a stored "0". The data stored in the chosen SRAM cell is subsequently indicated by the

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determined bit, which is then sent as an output. The waveform of the read operation is shown in Figure 3.

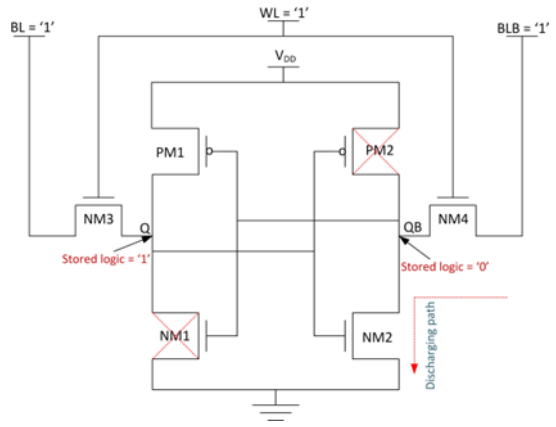

Figure 2. Read operation 6T SRAM Cell

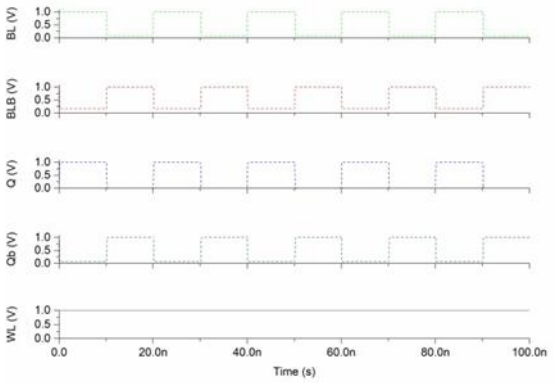

Figure 3. Resultant of Read operation 6T SRAM Cell

- Write mode: The write mode in a 6T SRAM cell is used to store or update data within the memory cell. Before a write operation, the bitlines (BL and BLB) are precharged to a certain voltage level, similar to a read operation. The wordline (WL) connected with the selected SRAM cell is turned on. This activates the access transistors, which connect the SRAM cell's storage nodes to the bitlines. In Figure 4 it shows the write operation in 6T SRAM cell.

In the write mode BL and BLB is charged to the Vdd. Once something is written in SRAM, either BL or BLB are discharged to the ground. If 1 is required to write, BL is charged to Vdd and BLB is discharged via ground. In the event where logic 0 is required to write, BLB charged to Vdd and BL discharged through ground, data is written into the cell and the WL becomes active. The SRAM cell's cross-coupled inverters stabilise in their new state, keeping the written data. The bistable feature of the latch ensures that the written information is retained in the cell until the next operation. The waveform of the write operation is shown in Figure 5.

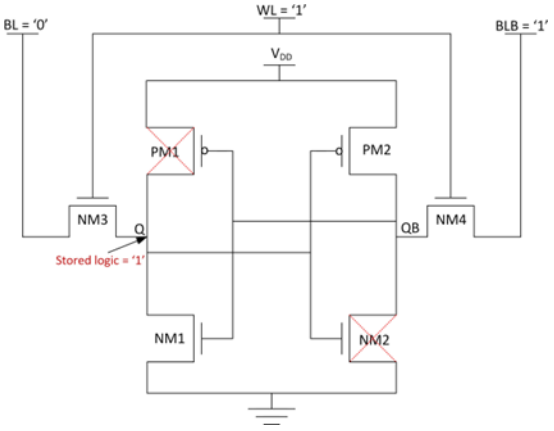

Figure 4. Write operation 6T SRAM Cell

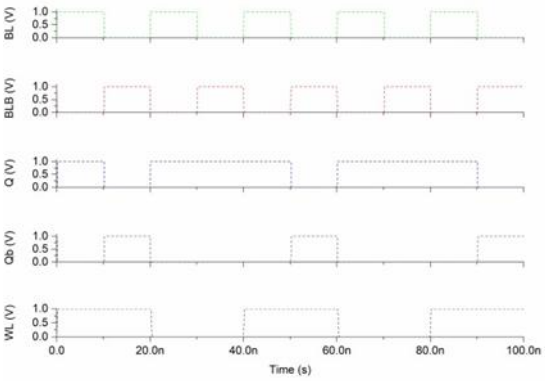

Figure 5. Resultant of Write operation 6T SRAM Cell

B. Stability

The terms "Read Stability" (RSNM) and "Write Stability" (WSNM) refer to the stability of read and write operations, respectively. The butterfly curve, which offers the circuit's static noise margin (SNM), is usually applied to calculate the stability of SRAM cells. RSNM can be determined by applying Vdd between pulldown transistors using dc analysis, in which case WL should be maintained high. The waveform can be generated by integrating the voltages at the storage node (Q or QB) and the bit lines (BL, BLB). Figure 6 show the RSNM through the butterfly curve.

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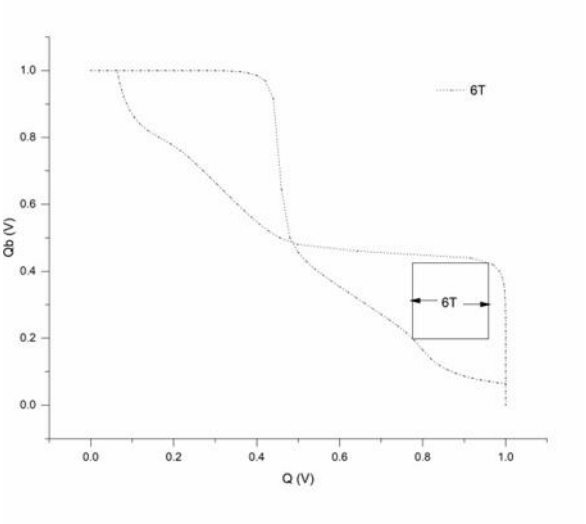

Figure 6. RSNM through butterfly curve

C. Soft Error Rate

Single-event upsets (SEUs) are occurrences generated by ionising radiation, such as cosmic rays, that can result in a temporary or permanent change in the state of a memory cell in CMOS (Complementary Metal-Oxide-Semiconductor) circuits. Ionising radiation's effects on the circuit's sensitive nodes are simulated when modelling SEUs. Injecting a double exponential current pulse at the sensitive nodes is a frequent way for simulating these effects. The supplied pulse has a brief rise time and moderate fall time. A double exponential current pulse is commonly used for modelling the SEU as well as calculating LET i.e Linear Energy Transfer[5].

(1)

In order to simulate the impact of a high-energy particle on the storage node, we used a double exponential current source model at sensitive node of the cell, where Qc is the critical charge, τα is the rise time constant (50ps) and τβ is the fall time (200ps) constant as suggest in [6,7].

The numerical integration of the current injected during the bit flip is used to compute the critical charge. (2)

+

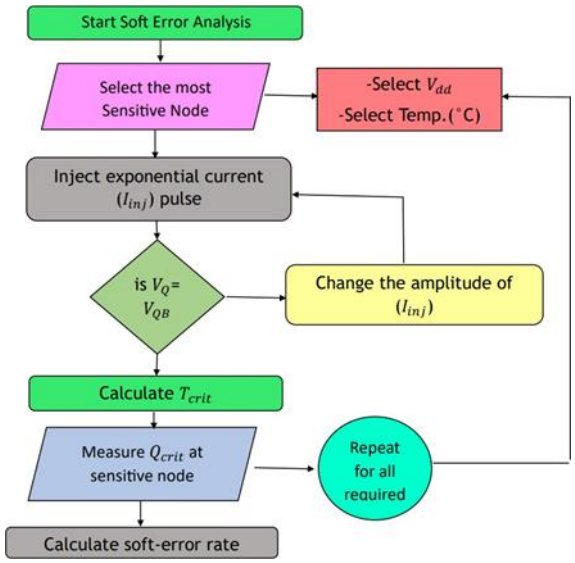

Figure 7. Simulation process for analysis of soft-error at different Vdd

[8].

Compared to the node holding "0," the node storing "1" is more susceptible to soft errors. Thus, when in standby state, I(t) injects node storing '1'. Amplitude of I(t) was changed in multiple simulation runs to find minimum current and minimal critical time Tc. The method used to compute soft error is shown in Figure 7. In Figure 8 it shows the flipping curve of 6T SRAM at storage QB of 1v and in Figure 9 it shows the non-flipping curve of 6T SRAM at storage QB of 1v.

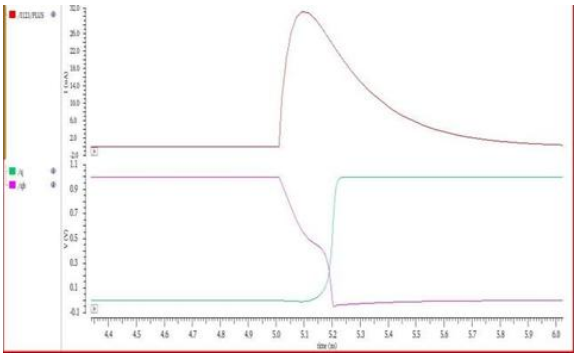

Figure 8. Flipping Curve of 6T at node QB of 1v.

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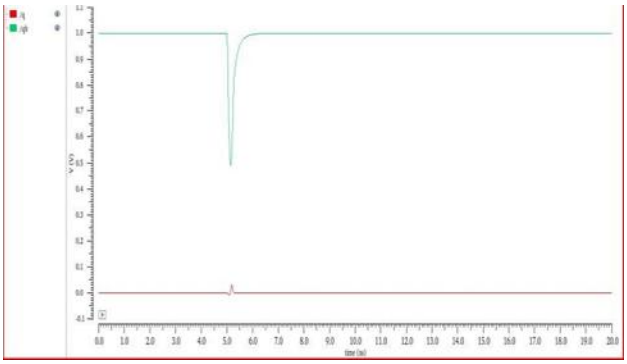

Figure 9. Non- Flipping Curve of 6T at node QB of 1v.

CONCLUSION

This paper presented a comprehensive analysis and simulation of a conventional 6T SRAM cell targeted for robust IoT-based applications. The design and evaluation were carried out using Cadence Virtuoso with GPDK 45 nm technology, focusing on read–write operations, stability, and radiation-induced soft error behavior. Detailed analysis of read and write functionality confirms correct operation of the memory cell, while stability was evaluated using Read Static Noise Margin (RSNM) through butterfly curve analysis.

Furthermore, the impact of ionizing radiation was analyzed by modeling single-event upsets (SEUs) using a double exponential current pulse, and the critical charge (Qcrit) was evaluated to assess soft error susceptibility. The simulation results demonstrate that the node storing logic '1' is more vulnerable to radiation-induced bit flips, highlighting a key reliability concern in nanoscale SRAM design.

Overall, the results indicate that the conventional 6T SRAM cell offers a good balance between performance, power efficiency, and area for IoT applications, but requires careful consideration of radiation effects in harsh environments. This study provides a strong foundation for future work on radiation-hardened SRAM architectures and assist techniques to further enhance reliability in next-generation low-power IoT systems

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