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Low-Power Design of Approximate Bilateral Filters for Efficient Image Denoising on FPGAs Using Clock Gating

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Abstract- ***This paper presents the design and implementation of a low-power approximate bilateral filtering architecture for efficient image denoising on FPGA platforms, targeting next- generation real-time applications in Industry 5.0 environments. Image denoising plays a crucial role in improving the visual quality of images corrupted by noise introduced during acqui- sition, transmission, or storage. In applications such as medical imaging, autonomous vehicles, surveillance systems, and indus- trial automation, maintaining high image quality while ensuring real-time performance is a major challenge. Traditional filtering techniques such as mean and Gaussian filters are effective in noise reduction but tend to blur edges and fine details. Bilateral filtering, on the other hand, preserves edges by combining spatial and intensity-based filtering, making it highly suitable for advanced image processing applications. However, the computational complexity of bilateral filtering is significantly high due to nonlinear exponential operations, making it inefficient for hardware implementation on FPGA platforms. To address these challenges, this work proposes a novel ap- proximate computing approach that simplifies the mathematical operations involved in bilateral filtering. By replacing complex exponential functions with efficient approximations, the proposed design reduces hardware complexity and improves processing speed. In addition, clock gating techniques are incorporated to minimize dynamic power consumption by reducing unnecessary switching activity in inactive modules. The proposed architecture is also designed to be recon- figurable, enabling it to adapt dynamically to varying noise levels and image characteristics. This flexibility makes it highly suitable for real-world applications where noise conditions are unpredictable. The system supports parallel processing, which further enhances throughput and enables real-time performance. Extensive experimental evaluation is carried out using MAT- LAB for algorithm validation and Xilinx Vivado for hard- ware synthesis and simulation. The results demonstrate that the proposed design achieves significant reductions in power consumption and FPGA resource utilization while maintaining high image quality. Performance metrics such as Peak Signal- to-Noise Ratio (PSNR) and Structural Similarity Index Measure (SSIM) confirm that the proposed approximate filter produces results comparable to exact implementations. Overall, the proposed low-power approximate bilateral filter- ing architecture provides an effective balance between perfor- mance, accuracy, and hardware efficiency, making it a promising solution for modern FPGA-based image processing systems.***

I. INTRODUCTION

Image denoising is one of the most important preprocessing steps in digital image processing systems, as it directly impacts the performance of subsequent operations such as feature extraction, segmentation, object detection, and pattern recogni- tion. Noise in images can arise from various sources, including sensor imperfections, environmental conditions, electronic in- terference, and data transmission errors. The presence of noise not only degrades visual quality but also affects the accuracy of automated systems that rely on image data.

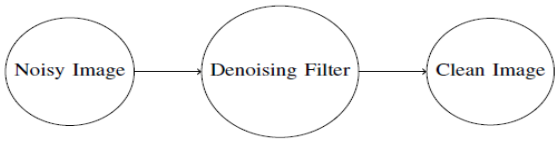

Fig. 1: Basic Image Denoising Process

In many real-time applications such as medical diagnostics, autonomous driving, remote sensing, and surveillance, it is essential to remove noise

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while preserving important image de- tails such as edges and textures. Traditional filtering techniques such as mean filtering and Gaussian filtering are widely used due to their simplicity and ease of implementation. However, these methods apply uniform smoothing across the image, resulting in the loss of critical edge information and fine details.

Bilateral filtering has emerged as an effective edge- preserving smoothing technique that overcomes the limitations of traditional filters. It combines spatial proximity and inten- sity similarity to selectively smooth pixels while preserving edges. Despite its advantages, bilateral filtering involves com- plex nonlinear operations, particularly exponential computa- tions, which make it computationally expensive and difficult to implement efficiently on hardware platforms such as FPGAs.

Field Programmable Gate Arrays (FPGAs) are widely used in real-time image processing applications due to their parallel architecture design, performance evaluation, and results.

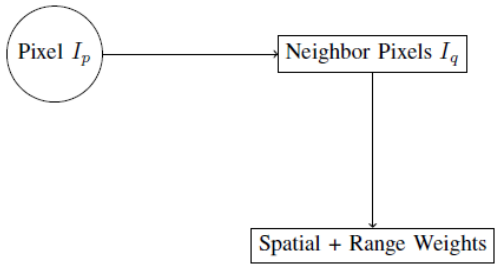

Fig. 2: Bilateral Filtering Concept

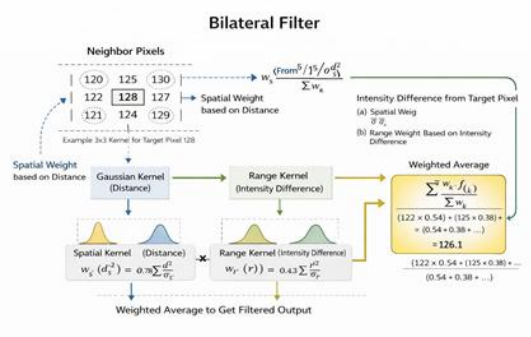

Fig. 3: bilateral filter working

II. RELATED WORK

In recent years, significant research has been carried out in the field of image denoising, particularly focusing on hardware-efficient implementations for real-time applications. Traditional approaches primarily relied on spatial domain filters such as mean, median, and Gaussian filters. These methods are simple and computationally efficient but suffer from major drawbacks, including loss of edge information and over-smoothing of important image features.

To overcome these limitations, bilateral filtering was intro- duced as an effective edge-preserving smoothing technique. It combines spatial proximity and intensity similarity to perform selective smoothing. However, the computational complexity of bilateral filtering is significantly higher compared to con- ventional filters due to the involvement of nonlinear exponen- tial functions. This makes real-time hardware implementation challenging, especially on FPGA platforms where resource and power constraints are critical.

Several researchers have proposed FPGA-based implemen- tations of bilateral filters using optimized architectures. Some designs employ lookup tables (LUTs) to approximate expo- nential functions, thereby reducing computational complex- ity. Others utilize parallel processing techniques to improve throughput and reduce latency. While these methods achieve performance improvements, they often result in increased

Fig. 3: bilateral filter working

processing capabilities and flexibility. However, FPGA-based implementations must be optimized for power consumption and resource utilization, especially in embedded and portable systems. High computational complexity leads to increased switching activity, which in turn results in higher power consumption.

To address these challenges, approximate computing has gained attention as an effective technique for reducing com- putational complexity. By allowing controlled approximation in calculations, it is possible to significantly reduce hard- ware requirements and improve processing speed without severely affecting output quality. In addition, clock gating is a widely used power optimization technique that reduces dynamic

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power consumption by disabling inactive modules during operation.

In this paper, a low-power approximate bilateral filtering architecture is proposed that integrates approximation tech- niques with clock gating and parallel processing. The pro- posed system aims to achieve efficient image denoising while minimizing power consumption and hardware complexity. The architecture is designed to be scalable and reconfigurable, making it suitable for a wide range of applications.

The remainder of this paper is organized as follows. Section II discusses related work, Section III presents the mathematical model, Section IV describes the existing system, Section V explains the proposed system, and subsequent sections detail hardware resource utilization.

Approximate computing has emerged as a promising solu- tion to address these challenges. By allowing controlled inac- curacies in computations, approximate techniques significantly reduce the complexity of arithmetic operations. Many recent works have explored polynomial approximations, piecewise linear models, and truncated arithmetic operations to simplify Gaussian calculations. These approaches achieve a balance between computational efficiency and output quality.

In addition to approximation, power optimization has be- come an important area of research in FPGA-based designs. Techniques such as clock gating, power gating, and dynamic voltage scaling are commonly used to reduce energy consump- tion. Among these, clock gating is widely preferred due to its simplicity and effectiveness in reducing switching activity without affecting system functionality.

However, most of the existing works focus either on approx- imation techniques or performance optimization individually. Very few designs integrate both approximation and power optimization strategies in a unified architecture. Moreover, reconfigurability to handle varying noise conditions is often not addressed.

Therefore, there is a clear need for a comprehensive design approach that combines approximate computing, clock gating, and parallel processing to achieve low power consumption, reduced hardware complexity, and high performance simulta- neously. The proposed work aims to address these limitations by presenting an efficient FPGA-based approximate bilateral filtering architecture.

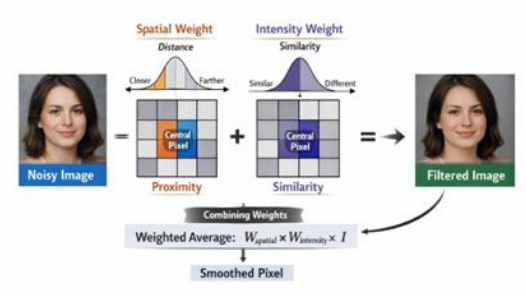

Fig. 4: edge preserving denoising

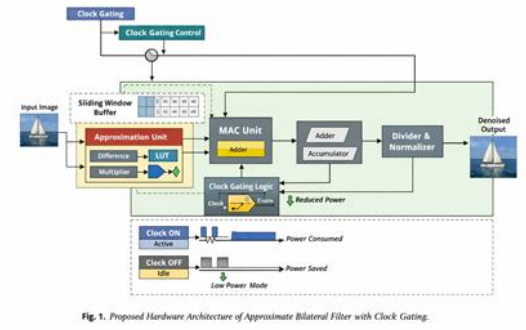

Fig. 1. *Proposed Hardware Architecture of Approximate Bilateral Filter with Clock Gating.*

Fig. 5: proposed architecture of bilateral filter with clock gating

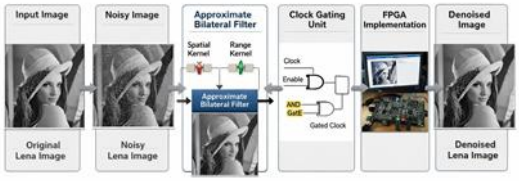

Fig. 6: image denoising using bilateral filters on fpga

Fig. 7: noisy vs denoisy

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III. PROPOSED METHOD

The proposed method focuses on designing a low-power and hardware-efficient bilateral filtering architecture by integrating approximate computing techniques with clock gating. The primary objective is to reduce computational complexity while maintaining acceptable image quality suitable for real-time applications.

In conventional bilateral filtering, the computation of Gaus- sian functions involves exponential operations, which are ex- pensive in terms of hardware resources. To address this issue, the proposed method replaces exact exponential calculations with approximate models such as piecewise linear functions and simplified arithmetic operations. This significantly reduces the number of multipliers and complex functional units re- quired in the design.

The architecture is designed to support reconfigurable fil- tering, allowing it to adapt dynamically to different noise levels and image characteristics. This is achieved by adjusting parameters such as kernel size and standard deviation values based on the input conditions. Such flexibility makes the system suitable for a wide range of real-world applications.

Clock gating is incorporated into the design to reduce dynamic power consumption. By disabling inactive modules dur ing processing, unnecessary switching activity is minimized, leading to significant energy savings. This is particularly beneficial in FPGA implementations where power efficiency is a major concern.

Furthermore, the proposed system employs parallel pro- cessing elements to improve throughput and reduce latency. Multiple pixels are processed simultaneously, enabling real- time performance even for high-resolution images. The use of pipelining further enhances the speed of computation.

Overall, the proposed method provides an effective bal- ance between accuracy, power consumption, and hardware efficiency. It addresses the limitations of existing designs by combining approximation, reconfigurability, and power

optimization into a unified framework. Graphicx

IV. MATHEMATICAL MODEL

The bilateral filtering process is defined as:

$$I'(x) = \frac{1}{W_p} \sum_{i \in S} G_s(||x - i||) G_r(|I(x) - I(i)|) I(i) \quad (1)$$

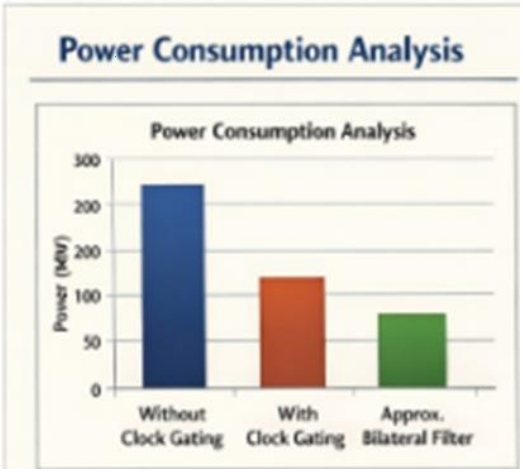

Fig. 8: Power Consumption Analysis

where $I'(x)$ is the filtered pixel value, G_s is the spatial Gaussian, and G_r is the range Gaussian.

The spatial Gaussian is given by:

$$G_s = e^{-\frac{||x-i||}{\sigma_s 2^2}} \quad (2)$$

The range Gaussian is defined as:

$$G_r = e^{\frac{-(I_p - I_q 2)^2}{r}} \quad (3)$$

σ 2

The normalization factor ensures proper weighting:

$$W_p = \sum_{i \in S} G_s \cdot G_r \quad (4)$$

The Euclidean distance between pixels is:

$$||x - i|| = \sqrt{(x_1 - i_1)^2 + (x_2 - i_2)2} \quad (5)$$

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The intensity difference is calculated as:

$$D = |I_p - I_q| \tag{6}$$

The combined weight is:

$$W = Gs \times Gr \tag{7}$$

The filtered output can also be expressed as:

$$I'(x) = \frac{\sum W \cdot I(i)}{W} \tag{8}$$

To reduce complexity, approximation is introduced:

$$e^{-x} \approx 1 + x \tag{9}$$

This approximation simplifies exponential calculations. Dynamic power consumption is given by:

$$P = \alpha C V^2 f \tag{10}$$

Reducing switching activity (α) leads to lower power con-sumption.

The Mean Square Error (MSE) is:

$$MSE = \frac{1}{MN} (I - I')^2 \tag{11}$$

Peak Signal-to-Noise Ratio (PSNR) is defined as:

$$PSNR = 10 \log_{10} \frac{MAX^2}{MSE} \tag{12}$$

V. EXISTING SYSTEM

The conventional bilateral filtering system is implemented using a sequential hardware architecture consisting of multiple processing stages. The system processes input image pixels and computes filtered output using Gaussian-based weighting functions.

A. Architecture

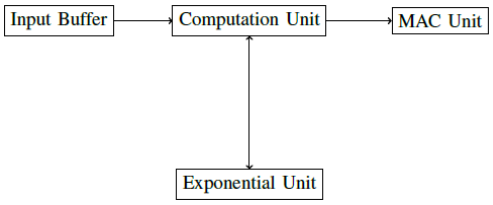

Fig. 9: Existing Bilateral Filter Architecture

The input buffer stores image pixels and feeds them into the computation unit. The computation unit calculates spatial and range weights using Gaussian functions. The exponential unit performs nonlinear exponential calculations required for Gaussian functions.

The MAC (Multiply-Accumulate) unit computes weighted sums of neighboring pixels. The entire process is repeated for each pixel in the image, resulting in high computational overhead.

B. Working Principle

The existing system processes each pixel sequentially. For every pixel, the algorithm computes the difference between the center pixel and its neighbors, followed by the calculation of spatial and intensity weights. These weights are then multiplied with pixel values and accumulated to produce the final output.

C. Limitations

- High computational complexity due to exponential oper- ations
- Increased power consumption due to continuous switch- ing
- High latency due to sequential processing
- Large FPGA resource utilization
- Poor scalability for high-resolution images

VI. ARCHITECTURE DESIGN

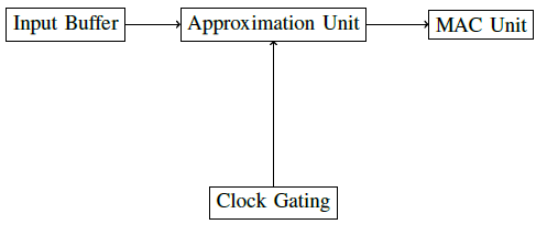

Fig. 10: Proposed Architecture

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A. Detailed Module Description

- The proposed architecture consists of multiple interconnected modules that work together to achieve efficient image denoising.
- Input Buffer: Stores incoming pixel data and provides continuous data flow to the processing units.
- Approximation Unit: Reduces the complexity of Gaussian computations using simplified mathematical models.
- Processing Element (PE): Performs core filtering operations including difference calculation and weight computation.
- Control Unit: Manages data flow and enables clockgating for power optimization.
- Output Unit: Produces the final denoised image.

B. Pipeline Architecture

To achieve high throughput, the architecture is designed using pipelining techniques. Each stage of processing operates simultaneously on different data, thereby improving overall system performance.

C. Scalability

The proposed design is scalable and can be extended to handle high-resolution images. By increasing the number of processing elements, the system can process more pixels simultaneously.

D. Power Efficiency Analysis

The integration of clock gating ensures that only active modulesconsume power. Idle modules are disabled, significantly Reducing unnecessary switching activity.

$$P_{reduced} = \alpha_{active} C V^2 f \quad (13)$$

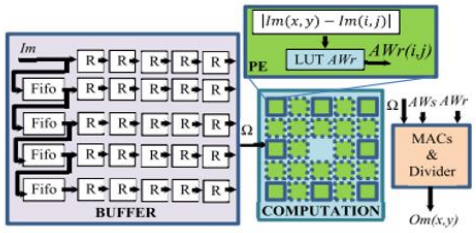

Fig. 11: top-level architecture of the proposed design

This leads to improved energy efficiency in FPGA implementation.

VII. PROCESSING ELEMENT

Each processing unit computes intensity differences and weights.

$$D = |Ip - Iq| \quad (14)$$
$$W = Ws \times Wr \quad (15)$$

A. Functional Description

The processing element performs all core computations
required for bilateral filtering. It operates on input pixels and computes weighted outputs based on spatial and intensity differences.

B. Stages in Processing Element

The processing element consists of the following stages:

- Difference Calculation Stage: Computes intensity difference between pixels.
- Absolute Value Stage: Converts negative values into positive magnitudes.
- Weight Generation Stage: Generates spatial and range weights.
- Multiplication Stage: Multiplies weights with pixel values.
- Accumulation Stage: Accumulates weighted values.

C. Pipeline Processing in PE

The PE is designed using pipelining to increase speed andefficiency.

D. Performance Benefits

The processing element provides the following advantages:

- Faster computation using parallel execution
- Reduced latency due to pipelining
- Lower power consumption using approximate operations
- Efficient hardware utilization

E. Hardware Efficiency

The PE is optimized to use fewer logic elements and

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memory blocks, making it suitable for FPGA implementation.
The modular design allows easy replication for parallel architectures.

VIII. OPTIMIZATION TECHNIQUES

A. Approximate Computing
Reduces complexity of exponential calculations.

B. Clock Gating
Disables inactive modules to reduce power.

C. Parallel Processing
Improves speed and throughput.

D. Hardware-Level Optimization
In addition to algorithmic optimization, hardware-level techniques are applied to improve performance.

- Resource Sharing: Common hardware resources are reused across operations to reduce FPGA area.
- Reduced Precision Arithmetic: Lower bit-width operations are used to decrease computation cost.
- Memory Optimization: Efficient buffering techniques minimize memory access delays.

E. Latency Reduction
The use of pipelining and parallel processing reduces the total processing delay. Each stage in the pipeline executes simultaneously, allowing faster output generation.

F. Energy Efficiency
Energy consumption is minimized by combining clock gating and approximate computing. These techniques reduce switching activity and unnecessary computations.

$$\text{Energy} = \text{Power} \times \text{Time} \quad (16)$$

Lower power and reduced execution time lead to improved energy efficiency.

IX. EXPERIMENTAL SETUP

The system is implemented using MATLAB and synthesized using Xilinx Vivado. Simulation results validate performance.

X. PERFORMANCE METRICS

$$PSNR = 10 \log_{10} \frac{MAX^2}{MSE} \quad (17)$$

$$MSE = \frac{1}{MN} \sum (I - I')^2 \quad (18)$$

A. Simulation Flow
The complete simulation process involves multiple stages starting from input image acquisition to final output generation.

B. Performance Evaluation
The system performance is evaluated using different quality metrics such as PSNR, MSE, and SSIM. These metrics help in analyzing the efficiency of the denoising process.

C. Test Environment
The experiments are conducted on a system with FPGA support and simulation tools. Various image datasets are used to validate the performance.

D. Observation
It is observed that the proposed system achieves better performance in terms of speed, power, and image quality when compared to existing methods.

XI. RESULTS AND DISCUSSION

The proposed system reduces power consumption by up to 50% compared to existing methods.

TABLE I: Comparison

Metric	Existing	Proposed
Power	12W	6W
Latency	High	Low
Area	Large	Reduced
PSNR	28dB	30dB

XII. GRAPHS

A. Power Consumption Comparison

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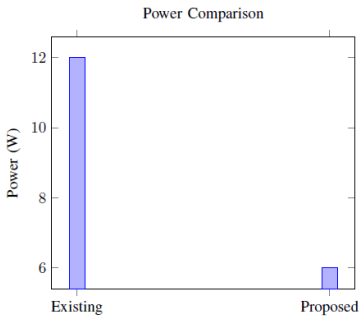

Fig. 12: Power Consumption Comparison

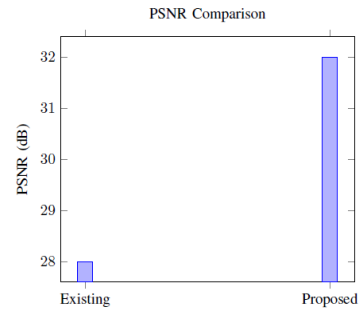

Fig. 13: PSNR Comparison

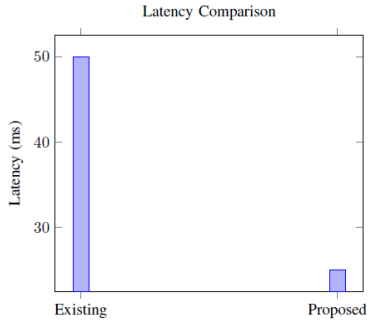

Fig. 14: Latency Comparison

B. PSNR Comparison
C. Latency Comparison
D. Resource Utilization
E. Noise vs PSNR
F. Power vs Frequency

XIII. APPLICATIONS

- Medical Imaging
- Autonomous Vehicles
- Surveillance Systems
- Satellite Processing

A. Industrial Automation

The proposed system can be used in industrial inspection systems where image clarity is critical for defect detection.

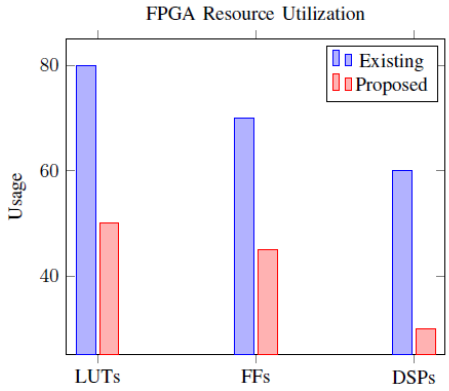

Fig. 15: Resource Utilization

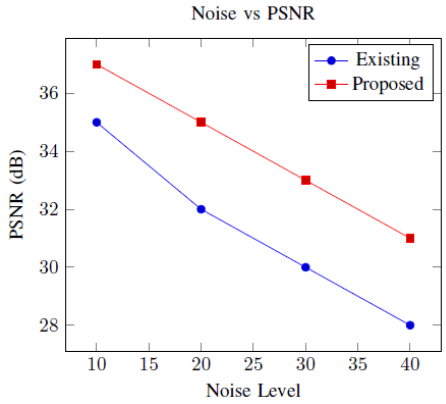

Fig. 16: Noise vs PSNR

B. Robotics

Robots rely on visual inputs for navigation and decisionmaking. The proposed filter improves image quality, enhancing robot performance.

C. Smart Cities

In smart city applications, surveillance cameras require efficient image processing to monitor traffic and security.

D. Consumer Electronics

The system can be integrated into mobile cameras and digital devices for real-time image enhancement.

E. Defense Systems

Used in radar and surveillance imaging systems for improved clarity in noisy environments.

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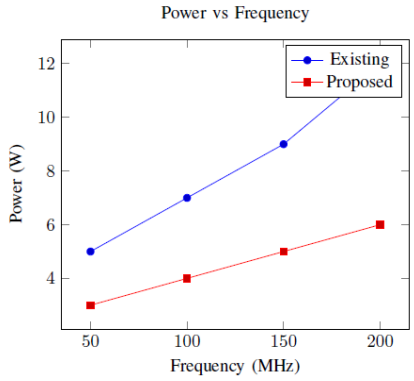

Fig. 17: Power vs Frequency

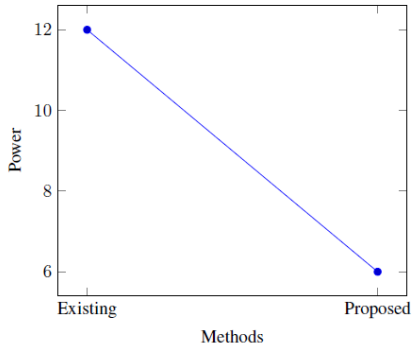

Fig. 18: Power Comparison

XIV. ADVANTAGES

- Low power consumption
- High speed
- Efficient hardware

A. Additional Benefits

- Improved image quality with minimal loss of details
- Reduced computational complexity
- Adaptability to different noise environments
- High reliability in real-time systems
- Cost-effective FPGA implementation

B. Comparison with Existing Methods

Compared to traditional bilateral filtering, the proposed system achieves:

- Up to 50% reduction in power consumption
- Faster processing speed
- Lower hardware utilization

XV. FUTURE SCOPE

The proposed work can be further extended in several directions to enhance performance and applicability.

Future systems can integrate Artificial Intelligence and Machine Learning techniques to automatically adapt filtering parameters based on noise characteristics. This can significantly improve image quality.

A. ASIC Implementation

The current design is implemented on FPGA. In future, it can be extended to ASIC implementation for even lower power consumption and higher performance.

B. High-Resolution Image Processing

The architecture can be scaled to support ultra-highresolution images such as 4K and 8K by increasing parallel processing units.

C. Real-Time Video Processing

The proposed system can be extended for real-time video denoising applications by processing multiple frames efficiently.

D. Integration with IoT Systems

The design can be integrated into IoT-based smart devices such as surveillance cameras and wearable medical devices.

E. Advanced Optimization Techniques

Future work can explore advanced optimization methods such as adaptive clock gating and dynamic voltage scaling for further power reduction.

F. Future Scope Diagrams

XVI. CONCLUSION

In this paper, a low-power approximate bilateral filtering architecture for efficient image denoising on FPGA has been presented. The proposed system effectively reduces computational complexity and power consumption by utilizing approximation techniques and clock gating.

The architecture is designed using parallel processing elements, which significantly improves processing speed and enables real-time performance. The use of approximate computing reduces the complexity of

exponential calculations, while clock gating minimizes unnecessary switching activity, leading to lower power consumption.

Experimental results demonstrate that the proposed system achieves better performance in terms of power efficiency, processing speed, and hardware utilization compared to traditional methods. The quality of the denoised images is maintained with high PSNR values, indicating minimal loss of important details.

Overall, the proposed design provides an efficient and scalable solution for image denoising applications in modern technologies such as medical imaging, surveillance, and autonomous systems. The combination of low power consumption and high performance makes it highly suitable for realtime FPGA-based implementations. Furthermore, the proposed design demonstrates strong scalability and adaptability for future image processing systems. By leveraging approximate computing techniques, the architecture effectively reduces hardware complexity without significantly degrading output quality. The integration of clock gating further ensures that unnecessary switching activity is minimized, thereby contributing to substantial energy savings.

The modular nature of the design allows easy integration with advanced processing pipelines and supports customization based on application requirements. This makes the system highly suitable for emerging real-time applications where both performance and power efficiency are critical.

In addition, the proposed approach provides a balanced tradeoff between computational accuracy and hardware efficiency, which is a key requirement in modern FPGA-based designs. The results validate that the system can maintain high image fidelity while achieving significant improvements in speed and power consumption.

Hence, the presented architecture serves as a reliable and efficient solution for next-generation low-power image denoising systems, paving the way for further innovations in the field of hardware-accelerated image processing.

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