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Analysis of Transient Voltage Protection in an 11 kV Protection Scheme: TVS Diode-Based Detection Technique

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Abstract- Transient overvoltages are primary cause of insulation stress, nuisance trips, misoperation of protective relays, and accelerated aging in medium-voltage (MV) networks. Analysis of transient voltage phenomena in an 11 kV distribution environment and development of a TVS (Transient Voltage Suppressor) diode-based detection technique that complements standard surge protection (e.g., metal-oxide varistors, gas discharge tubes) and conventional protection schemes (overcurrent, earth fault, distance, differential) is covered in this paper. The proposed approach uses a high-impedance, galvanically isolated measurement path and TVS diodes in a low-energy, secondary detection channel to reliably flag fast-rising transients (e.g., lightning-induced surges, switching events) without imposing additional stress on primary equipment insulation. The architecture integrates three cascaded domains: transformer-based galvanic isolation, signal conditioning with transient voltage suppression (TVS) clamping, and asynchronous comparator thresholding. Simulation results confirm that the SMBJ6.0A TVS diode enters avalanche breakdown within picoseconds, while the TLV2372D comparator produces sharp digital transitions with sub-microsecond propagation delay. Although theoretical hardware contributions yield a response latency of ~1.5 µs, system-level simulations demonstrate a measured response time of 9 µs, dominated by transformer and rectifier dynamics. When interfaced with microcontroller hardware interrupts, the additional MCU latency of 0.5 µs is negligible, resulting in a total trip time of 9.5 µs. These findings validate the superiority of hardware-driven detection over software polling, offering deterministic, ultra-fast protection suitable for breaker trip signaling in high-voltage substations.

Keyword: 11 kV MV Distribution, Transient Overvoltages, Surge Detection, TVS Diode, Galvanic Isolation, Avalanche Breakdown, Potential Transformer (PT), Comparator Thresholding, Response Latency, Microcontroller Interrupts, Signal Conditioning.

I. INTRODUCTION

Transient overvoltages in MV systems stems from sources like lightning, capacitor bank switching, vacuum breaker current chopping, and ferroresonance (Baitch, 2000; Greenwood, 1991; IEEE, 2024). They can produce steep-front waveforms that stress insulation systems and protection devices (IEC, 2018). In 11 kV networks common to industrial plants and offshore facilities, these events may cause degradation in cable terminations, bushings, and instrument transformers, while also inducing nuisance trips or mal-operations in protective relays and control electronics (IEC, 2018; Stone et al., 2014).

Conventional protection frameworks emphasize primary energy handling (surge arresters based on MOVs, occasionally with GDTs and coordinated spark gaps) and fault clearing (overcurrent, earth fault, distance, differential) (Blackburn and Domin, 2014; IEC, 2014). However, many installations lack a high-fidelity, fast transient detection channel that (i) discriminates fast transients from PF disturbances (Bollen, 2000), (ii) timestamps and classifies events for asset health analytics (Stone et al., 2014), and (iii) feeds adaptive protection logic without adding appreciable loading to the bus.

This paper proposes and analyzes a TVS-diode-based detection technique integrated into an 11 kV scheme. Recognizing that TVS diodes are not suitable for dissipating MV transient energy directly, we deploy them in a secondary, isolated, stepped-down measurement path where their steep front sensitivity and nanosecond-scale clamping behavior act as an effective surge discriminator when combined with suitably designed RC networks, isolation, and signal conditioning. The result is a robust, low-latency trigger for transient logging and supervisory protection features, that will improve visibility and enable condition-based maintenance.

II. BACKGROUND AND RELATED WORK

A. Transient Sources in 11 kV Systems

Primary sources of transients include:

i. Switching operations: These include capacitor banks, reactor switching, and transformer energization, which can produce high $\frac{dV}{dt}$ and restrikes (Greenwood, 1991).
ii. Lightning-induced surges: The surges can couple into overhead lines or enter via transformer HV terminals.
iii. Vacuum interrupter current chopping and Transient Recovery Voltage (TRV) across breakers.
iv. Ferroresonance: This can occur in lightly loaded PT circuits and cable-transformer combinations.

These cause steep-front traveling waves which are partially mitigated by surge arresters, line terminations, and insulation coordination practices. Yet, awareness of event frequency, magnitude, and location often remains limited, making detection valuable for maintenance planning and protection tuning.

B. Surge Protection Elements

MOV Arresters: The primary function is to defend against high-energy transient overvoltage across incoming feeders, transformer HV terminals, and selected bus locations. The arrester achieves this by rapidly transitioning from a high-resistance to a highly conductive state to safely clamp excessive voltage (IEC, 2014).

GDTs: Uses a sealed, gas-filled chamber and coordinated spark gaps to protect sensitive infrastructure from extreme surge currents in specialized applications. When a transient voltage exceeds the breakdown threshold, the internal gas or air gap ionizes, creating a low-impedance path that effectively shorts the destructive energy to ground (Greenwood, 1991).

RC Snubbers: This involves placing a capacitor and resistor across breaker contacts to Suppress high-frequency, transient overvoltage caused by current chopping or contact restrikes during inductive or capacitive load switching. The capacitor (C), absorbs and stores the high-frequency energy of the transient, altering the natural frequency of the local circuit to significantly slow down the voltage rise time. While the resistor (R), provides critical damping to dissipate the trapped high-frequency energy as heat, effectively preventing continuous resonant oscillations between the line inductance and the circuit capacitance (Greenwood, 1991).

Line Traps and Damping: Act as a high-frequency parallel resonant (LC) filter inserted into high-voltage transmission lines. They present negligible impedance to the standard power frequency (e.g., 50 Hz or 60 Hz), allowing power to pass freely, while presenting high impedance to high-frequency transient signals. The damping element typically uses heavy-duty resistors connected in parallel to the main tuning device to suppress voltage spikes and prevent hazardous resonant oscillations triggered by lightning, switching operations, or system faults. They dissipate the energy of high-frequency transients, safeguarding downstream protective relays and instrumentation (Anderson, 1999; IEEE, 2003).

C. TVS Diodes in Medium-Voltage Protection Schemes

TVS Diode:
This is a specialized solid-state, PN-junction semiconductor device designed specifically to protect sensitive electronic components from sudden voltage spikes and transient overvoltage events such as ESD (Electrostatic Discharge) strikes, inductive load switching, or lightning surges.

Unlike standard rectifying diodes or Zener diodes, which are designed for continuous current conduction and voltage regulation, a TVS diode is engineered to operate as a high-speed, heavy-duty safety switch.

TVS diodes are typically connected in parallel with the protected circuits and in a reversed direction. It can operate in unidirectional or bidirectional configurations (He et al., 2022). Under normal operating conditions, the TVS diode remains invisible to the circuit. It acts as an open circuit with high impedance and minimal leakage current. However, its behavior changes instantly when a voltage spike occurs.

Figure 1: Bidirectional and unidirectional TVS diodes

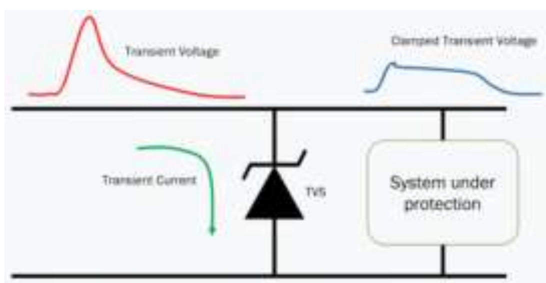

Figure 2: TVS Diode Operation and Voltage Clamping Profile. (Image source: Micro Commercial Components)

When surge occurs, whereby the voltage exceeds the predetermined threshold the TVS diode detects this change in nanoseconds, then clamps to divert the large portion of the voltage away from the circuit (Van and Venter, 2025). The excessive transient current flows through the TVS back to the source, ensuring constant voltage for the protected system. After the surge is over, the TVS diode will automatically reset to its non-conducting state, ready to protect the circuit from the next unexpected surge.

These critical parameters define the performance of TVS diode:

Reverse Stand-Off Voltage (VRWM): The maximum continuous operating voltage the diode can withstand without turning on. Below this threshold, the diode remains in its high-impedance 'off' state (STMicroelectronics, 2018).

Breakdown Voltage (VBR): The specific voltage at which the diode begins to conduct and enter avalanche breakdown. It is typically measured at a standard test current (e.g., 1 mA) (ON Semiconductor, 2004).

Clamping Voltage (VC): The maximum voltage drop across the diode when it is carrying the full rated peak pulse current (IPP). This represents the maximum voltage stress the downstream circuit will face during a surge (ON Semiconductor, 2004).

Peak pulse current (IPP): Is the maximum surge current specified for the device.

Reverse leakage current (IR): Which is the current measured at VRWM.

Test current (IT): Which is the current at VBR
Response Time (tr): The time it takes for the diode to react to an overvoltage event. For silicon TVS diodes, this is virtually instantaneous (typically <1 picosecond for unidirectional variants and <1 nanosecond for bidirectional variants) (Eaton, 2020).

Illustration of the key device parameters of TVS diodes is as shown in Figure 3.

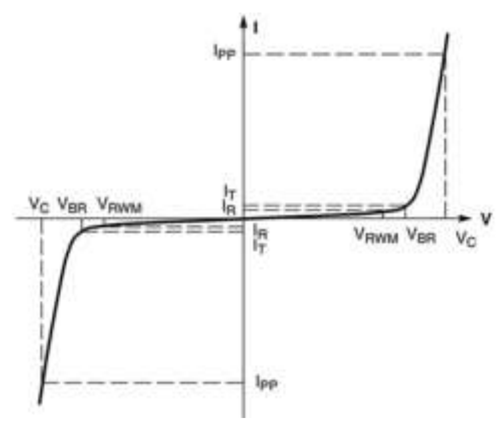

Figure 3: Voltage/current characteristic for bidirectional TVS diodes (Image source: ON Semiconductor)

The graph plots current (I) versus voltage (V) to show how the device behaves during normal operation and overvoltage surges. The graph maps crucial operational thresholds that determine how effectively the device shunts spike energy to ground. The visual profile of the graph changes depending on whether the TVS component is unidirectional or bidirectional (ON Semiconductor, 2004).

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Integration and Scalability of TVS Diodes in MV System:

TVS diodes are widely used in low-voltage electronics for ESD and surge clamping. In MV power systems, a direct connection of TVS diodes to 11 kV buses is not advisable due to insulation, creepage/clearance distance, and thermal/energy constraints. However, when placed behind an appropriate scaling and isolation chain like potential transformer (PT) or Resistor-Capacitor (RC) divider, TVS diodes can serve as ultra-fast threshold detectors, providing clean logic transitions that mark the arrival of impulsive transients. This move from energy absorption to event detection is the key innovation explored in this paper. Recent research has advanced the understanding of transient voltage suppression in medium-voltage systems, with particular emphasis on semiconductor-based protection devices. Gupta and Patel (2021) analyzed common-mode faults in transformer-isolated power systems, underscoring the importance of galvanic isolation in preventing fault propagation into downstream electronics. Their findings support the use of cascaded transformer networks in detection architectures.

Building on material science innovations, Zhang and Li (2020) investigated silicon carbide-based TVS devices, demonstrating enhanced clamping performance and resilience under high-energy surges. Extending this line of inquiry, He et al. (2022) introduced a novel AlGaN/GaN transient voltage suppression diode with bidirectional clamp capability, achieving nanosecond-scale response times. These studies highlight the potential of advanced semiconductor materials to improve surge discrimination in MV environments.

At the circuit design level, Lee and Park (2021) focused on high-speed comparator design for transient detection in power electronics, showing how optimized thresholding circuits can achieve sub-microsecond response times. Their work directly informs the comparator-based architecture integrated into TVS diode detection schemes. Complementing this, van Niekerk and Venter (2025) conducted reliability analysis of TVS diodes under direct current switching surge stress, providing critical insights into endurance and failure mechanisms under repeated transient exposure.

Together, these contributions establish a foundation for the present study. While conventional MOV arresters and GDTs remain widely deployed, recent literature emphasizes the limitations of traditional devices in dissipating steep-front transients. The integration of TVS diodes into stepped-down, isolated measurement paths represent a novel approach, leveraging their picosecond clamping behavior for event logging rather than bulk energy absorption. This research therefore extends the state of the art in transient voltage protection for 11 kV schemes by synthesizing insights from transformer isolation, comparator optimization, and advanced TVS materials.

III. DETECTION TECHNIQUE DESIGN METHODOLOGY

The proposed high-speed detection technique follows a strictly linear, decoupled topology engineered to translate high-energy, primary-side medium-voltage anomalies into low-voltage digital events. The architectural design is in procedural stages, culminating in a critical data output loop.

A. System Architecture and Operational Design

To overcome the physical, insulation, and thermal limitations of applying solid-state semiconductors directly to MV systems, a multi-stage conditioning, decoupling, and high-speed detection topology was designed and simulated using Proteus Design Suite. The system converts primary 11 kV line dynamics into low-voltage, galvanically isolated digital logic edges optimized for real-time microchip interruption.

The structural architecture is divided into three cascaded domains: Primary Volumetric Sensing, Analog Waveform Conditioning & Clamping, and Asynchronous Threshold Comparison.

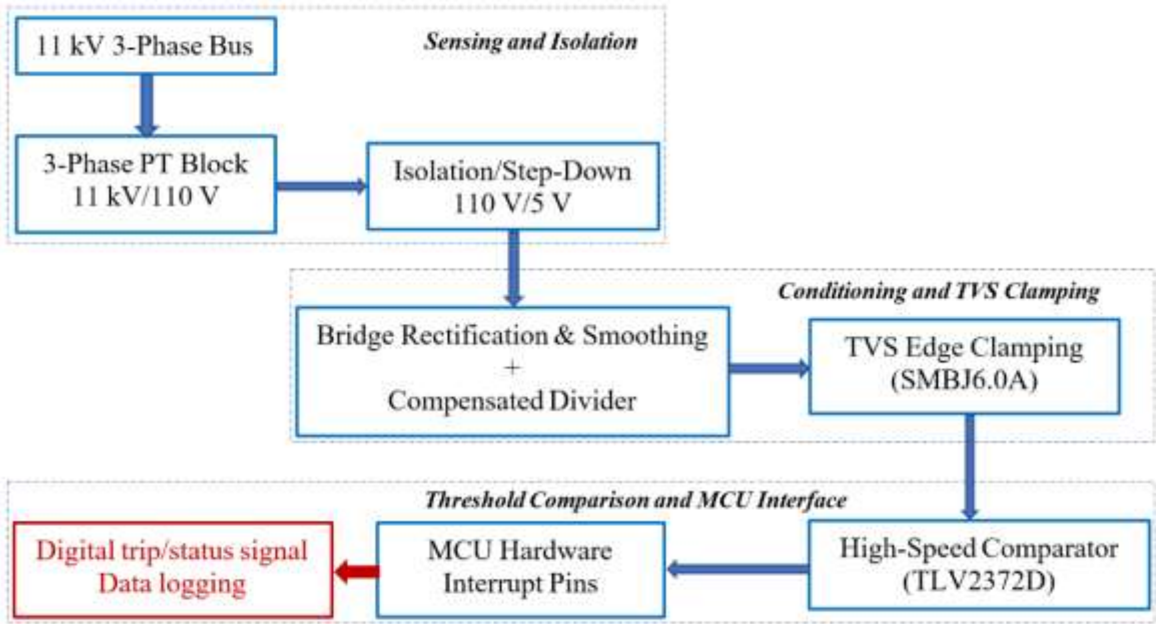

Figure 4: Block diagram of TVS-based high-speed transient detection system architecture

Sensing and Galvanic Isolation Stage:
The front-end interface connects directly across the 11 kV three-phase network. Raw transient energy is mitigated immediately via a multi-stage transformer network, because there is to strict adherent to basic insulation level (BIL) and creepage requirements in transformer structure (IEEE Std 1427-2020; Vyas, 2026). The 3-phase PT Functions as the primary boundary layer, stepping down the 11 kV line-to-line voltage to a safe, measurable 110 V, low-voltage AC baseline while providing primary galvanic isolation. Each individual phase is routed through dedicated step-down isolation transformers (for Phase A, Phase B, Phase C). This arrangement steps the 110 V to 5 V AC while establishing separate phase-isolated secondary loops, ensuring that common-mode faults or ground-loop noise cannot propagate into downstream instrumentation electronics (IEEE Std 1100-2022; Kong and Chen, 2025).

Signal Conditioning and TVS Clamping Stage:
After stepping down from MV to a low-voltage AC, the signal enters the conditioning stage to convert the AC wave into a unipolar DC monitoring profile. Each phase utilizes Full-Bridge rectifier, and parallel damping resistors and electrolytic capacitors that smoothens the rectified output, establishing a highly stable, scaled DC proportional to the peak voltage of each respective phase. The rectified DC link is applied across a voltage divider to bring the steady-state nominal operational voltage within the sensing thresholds of the active logic chips (Kaunkid et al., 2024).

The TVS diode sits safely below its reverse stand-off voltage (VRWM) under normal 11 kV line conditions, leaving it in a high-impedance, transparent state. During high - $\frac{dV}{dt}$ transient overvoltage event that penetrates the transformers, the scaled analog voltage sweeps past the breakdown voltage (VBR) (Lee and Park, 2021). The TVS diode instantly enters avalanche breakdown within picoseconds, clamping the maximum voltage exposure across the comparator input to a rigid, safe clamping profile (VC), as shown in Figure 3.

Threshold Comparison and MCU Interfacing:
This architecture directs the TVS-clamped node into a hardware-driven comparison circuit rather than going straight to the Analog-to-Digital Converter (ADC) built into the MCU. The clamped sensing junction is fed into the non-inverting input (IN+) of a low-power, high-speed operational amplifier configured as an overvoltage comparator. The inverting terminal (IN-) is locked to a highly precise reference voltage representing the overvoltage fault threshold. The instant a fast transient wave causes the non-inverting input to cross the reference voltage boundary, the comparator output snaps to its saturation rail, generating an ultra-sharp,

near-vertical square logic transition edge (Lee and Park, 2021; Texas Instruments, 2023).

The outputs of the comparators are passed through isolating series-termination resistors and pulling networks to give discrete digital outputs of 5 V DC to be routed directly to the hardware interrupt pins of an MCU.

By bypassing MCU's sequential software execution loops and software-based RMS polling, the occurrence of an overvoltage transient trigger a direct and instantaneous asynchronous hardware interrupt. This architecture shifts the primary role of the solid-state TVS diode from standard thermal energy destruction to ultra-fast event logging and microsecond-level breaker trip signaling

B. Hardware Schematic Design and Simulation Topology

To validate the high-speed transient detection methodology, a complete multi-phase electronic schematic was designed and simulated within the Proteus Design Suite environment. The simulation topology is structured to model everything from the MV mains down to the MCU digital interface, proving the feasibility of the signal-conditioning hardware.

Primary MV Generation and Galvanic Isolation Modeling:

The left-hand sector of the simulation topology establishes the medium-voltage boundary layer. A three-phase power source (11 KV 3PH MAINS) represents the nominal steady-state utility grid supply. This is followed by stage of the schematic that handles voltage step-down and galvanic safety isolation

i. To simulate real-world substation load dynamics, a heavy industrial inductive consumer (11 kV MOTOR) is tied in parallel to the main incoming feeder lines.
ii. Isolation and switching control are simulated via a high-voltage three-phase circuit breaker network (MV1), which allows the investigation of both steady-state operations and transient switching abnormalities (such as current chopping or contact restrikes) within the software model.
iii. Alternating current (AC) voltmeters are mapped across each line-to-ground path to continuously monitor the primary 11kV voltage scaling profile.
iv. The primary 11 kV lines are scaled down to 110 V by a central three-phase PT (TRAN-3PHASE). To prevent hazardous common-mode noise and ground loops from feeding forward into the computing electronics, each phase is assigned an independent step-down isolation transformer (X1, X2, and X3) (Gupta et al., 2021). These transformers step the voltage down further to a low-energy, instrument-safe 5 V AC baseline.

To reduce MV input to safe secondary voltage.
11 kV → 110 V → 5 V
For the step-down isolation transformer X1, X2, and X3

$$V_{s(peak)} = V_{sec} \times \sqrt{2} \quad (1)$$

Input voltage (V_{pri}): 110 V RMS

Output voltage (V_{sec}): 5 V RMS

Turns ratio:

$$K_n = V_{pri}/V_{sec} \quad (2)$$

Peak secondary voltage:

$$V_{s(peak)} = V_{sec} \times \sqrt{2} \approx 7.07 \text{ V}$$

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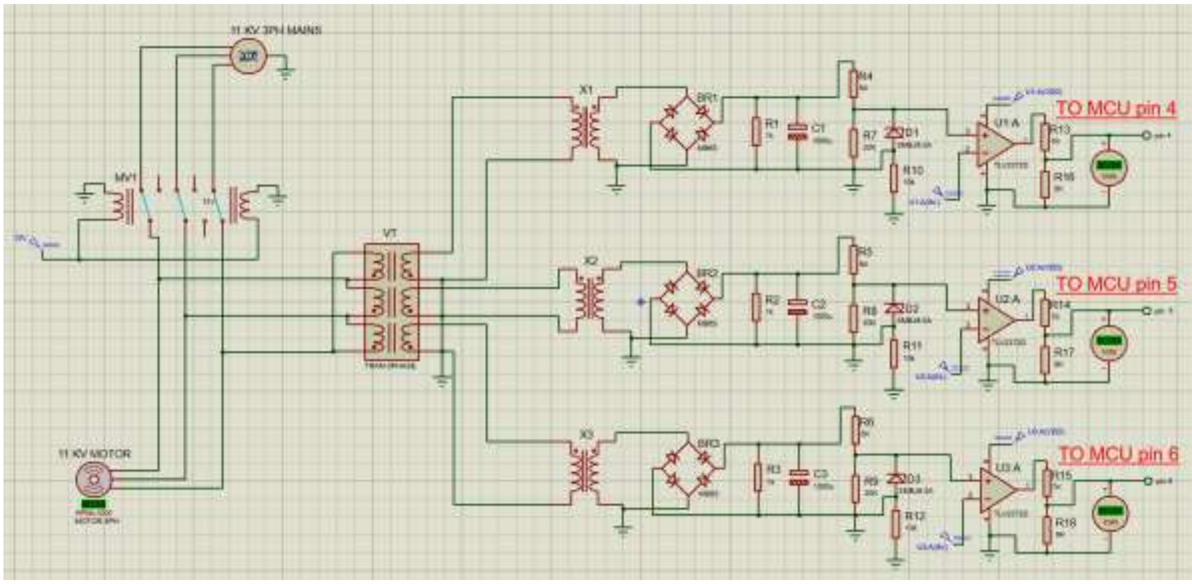

Figure 5: Complete schematic diagram of the three-phase TVS-based transient overvoltage detection circuit.

Signal Conditioning and TVS Overvoltage Clamping:
The intermediate stage of the schematic handles unipolar wave reshaping and the detection system, limiting analog overvoltage to a safe profile for the high-speed intelligent circuit. The three phases follow identical, symmetrically decoupled hardware paths to ensure uniform response timing.

i. Rectification and Smoothing Capacitor: Each secondary loop passes through a dedicated high-speed switching Schottky bridge rectifier, MB6S. A parallel damping resistor (1k) and a massive electrolytic filtering capacitor (1000uF) act as a smoothing capacitor. This stage effectively converts the raw AC secondary into a highly responsive, unipolar DC envelope that linearly tracks the true root-mean-square (RMS) and peak fluctuations of the primary 11 kV grid.

ii. The TVS Sensing Node: The smoothed DC voltage is dropped across a precision compensated voltage divider network (R4 = 5k and R7 = 20k) (Kaunkid et al., 2024). Anchored securely across the lower arm of this divider is a solid-state TVS diode (SMBJ6.0A). Under nominal grid voltages, the scaled analog voltage remains well below the diode's 6.0V reverse stand-off threshold, allowing the diode to remain in a transparent, passive state. However, the moment an external surge or steep-front switching overvoltage event penetrates the transformer chain, the voltage exceeds this threshold. The TVS diode undergoes instantaneous avalanche breakdown, clamping the analog voltage to a safe, fixed profile (VC) and absorbing low-energy transient remnants (Zhang and Li, 2020; Texas Instruments, 2020). The absorbed energy is limited to ground through 10k resistor (R10, R11, R12).

With respect to Figure 5, the mathematical model is as follows:

To Convert AC to DC using full-wave bridge rectifier (Boylestad et al., 2013):

$$V_{dc(peak)} = V_{s(peak)} - 2V_f \qquad (3)$$

Bridge rectifier, $V_f \approx 1.0$ V

Two diodes conduct per cycle

Peak rectified voltage:
$V_{s(peak)} = 5$ V RMS $= 5 \times \sqrt{2} = 7.07$ V
$V_{dc(peak)} = V_{s(peak)} - 2V_f \approx 5.07$ V
To Smoothen the pulsating DC with capacitor (Boylestad et al., 2013):

$$V_{ripple(p\text{-}p)} = I_L / (f_r \times C) \qquad (4)$$

Capacitor C1: 1000 μF

Ripple frequency: $f_r = 2f_{in} = 100$ Hz

Ripple voltage: $Vr = I_L / (f_r \times C)$

Average DC output:

$VDC = Vdc(peak) – V_r / 2$ (5)

The scale DC voltage for comparator non-inverting input (Kaunkid et al., 2024):

$V_{out} = VDC × R7 / (R4 + R7)$ (6)

Divider resistors: R4 = 5 kΩ, R7 = 20 kΩ

With given values: Vout = VDC × 0.8 ≈ 4.5 V

Threshold Comparison and MCU Interfacing:

The final stage of the hardware schematic constitutes the core high-speed intelligence of the detection system, turning analog overvoltage behavior into immediate digital actions.

i. High-Speed Comparator Interface: The clamped junction is continuously monitored by a TLV2372D operational amplifier configured as an active overvoltage comparator (U1:A, U2:A, U3:A). The non-inverting pin (IN+) receives the dynamic voltage signal from the TVS node, while the inverting pin (IN-) is bound to a highly stable, fixed DC voltage reference (6 V) (Texas Instruments, 2020).

ii. Digital Output Transition: The moment the non-inverting input crosses the reference voltage boundary, the comparator output instantly saturates to its positive rail (12V DC). This transition is sharpened into a crisp, vertical logic step edge. The resulting signal passes through voltage divider networks (R13/R16, R14/R17, R15/R18) to emerge as independent digital outputs routed directly to the microcontroller's hardware interrupt pins (TO MCU pin 4, pin 5, and pin 6) (Kaunkid et al., 2024).

With respect to Figure 5, the mathematical model is as follows:

To establish stable comparator reference with the TVS diode:

Supply voltage: VDD = 12 V

TVS diode D1: SMBJ6.0A, Breakdown voltage (VBR) = 6.7 V (Texas Instruments, 2020)

$I_{BR} = (VDD – VBR) / R10$ (7)

Resistor R10 = 10 kΩ controls I_{BR}

$I_{BR} = (VDD – VBR) / R10 \approx 0.53$ mA

To compare sensed voltage against reference:

If $V_{sense} < V_{ref}$, $V_{out} = 0$; (8)

else $V_{out} \approx VDD$

$V_{sense} = V_{rectified} × (R7 / (R4 + R7))$ (9)

$V_{sense} = V_{rectified} × (20k/(25k)) = 0.8 × V_{rectified}$

$V_{ref} = 6.0$ V, $V_{pin3} = 6.7$ V

Since $V_{pin3} > V_{pin2}$, comparator saturates to VDD

To ensure safe 5 V logic level for MCU:

$V_{final} = V_{pin1} × R16/(R13+R16)$ (10)

Divider resistors: R13 = 7 kΩ, R16 = 5 kΩ

$V_{final} = V_{pin1} × (R16 / (R13+R16))$

With $V_{pin1} \approx 12$ V, $V_{final} \approx 5$ V

IV. RESULTS AND DISCUSSION

A. Simulation Setup and Parametric Test Conditions

i. Normal Operating Baseline: The steady state voltage is 11 kV AC, which is scaled to 110 V AC then to 5 V AC and finally to DC voltage that sits safely below the 6.7 V DC TVS threshold with no transient pulse generated, as shown in the graph of Figure 6. The AC sinewave (BLUE) is the AC scaled signal at the secondary output of isolation transformer X1, X2, X3. The rectified DC signal (GREEN) is at the TVS node. The pulse signal (RED) is the logic output of the comparator through the voltage divider network. Figure 6 shows the waveforms at normal operating baseline.

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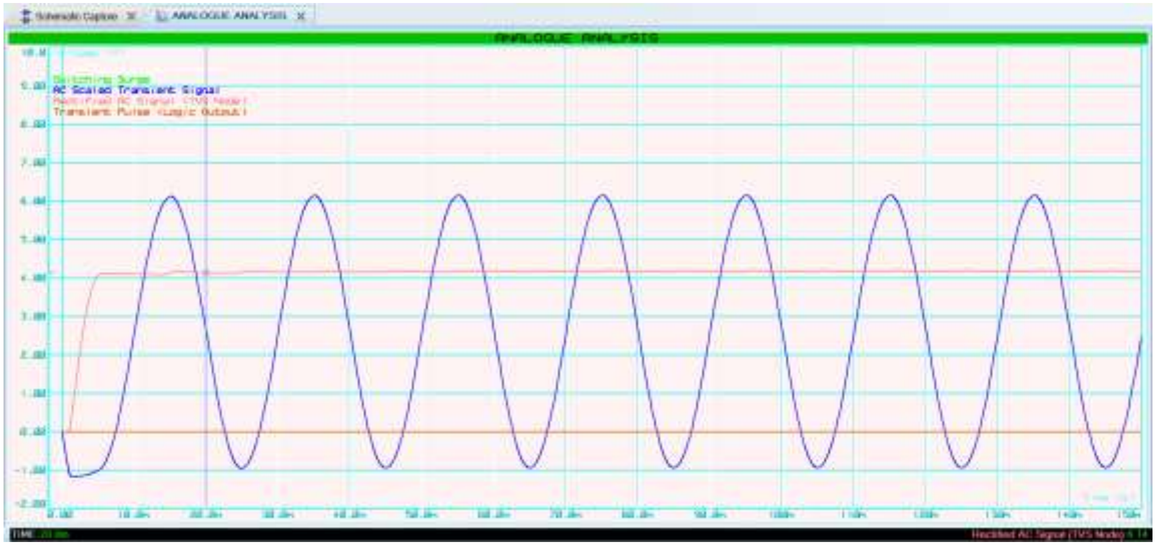

Figure 6: Signal waveforms at normal operating baseline.

ii. Transient Generation: The transient overvoltage event was introduced by applying a piecewise linear signal (PWLIN) of about 21 kV with a rise time of 1 µs to the 11 kV steady state sinusoidal signal, to mimic switching surges from opening/closing MV1.

B. Waveform and Performance Analysis

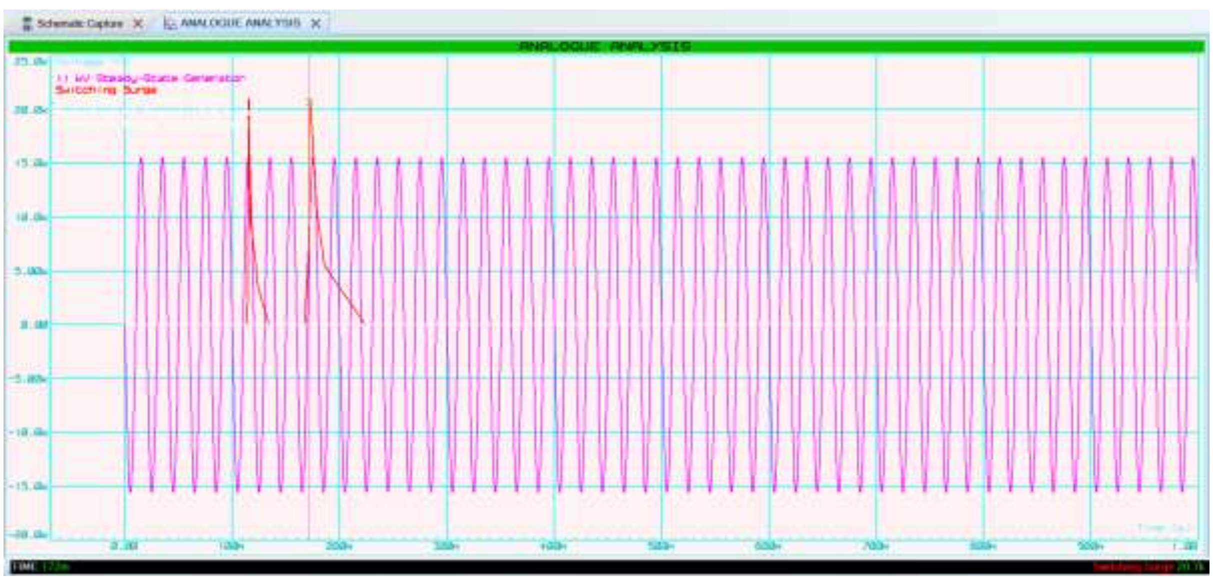

Figure 7: Waveform of the switching surges on the steady state signal.

Figure 7 shows the instance the switching surges with amplitude up to 21 kV acted on the steady state nominal source. Figure 8 shows the steady state 11 kV nominal gave equivalent of 4.33 V RMS with peak voltage of 6.12 V AC (BLUE), which represents the AC scaled signal at the secondary of isolation transformer X1, X2, X3. The TVS diode successfully clamped the rectified DC signal to 6.66 V DC (GREEN) after entering avalanche breakdown and flattening the spike. At the instance of clamping the transient overvoltage, the comparator gave an instantaneous interrupt pulse of 5 V DC (RED) after threshold hold comparison by snapping from 0 V to 5 V logic High.

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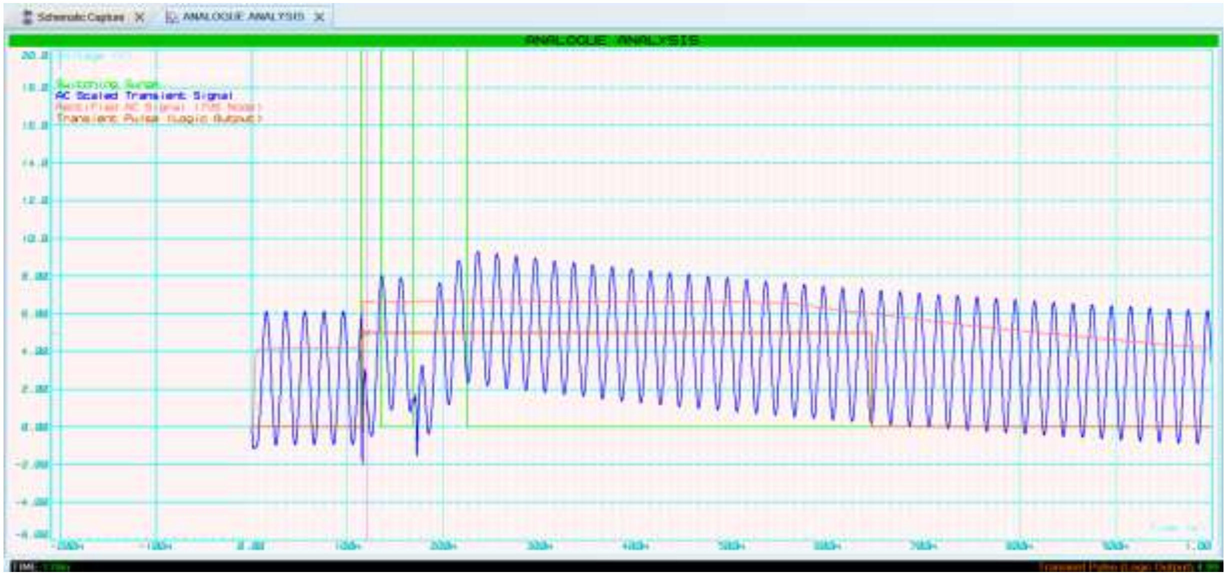


Figure 8: Signal waveforms at transient overvoltage event.

i. Latency Evaluation and Response Time Calculations

To calculate the total response latency Δt from the simulation plots:

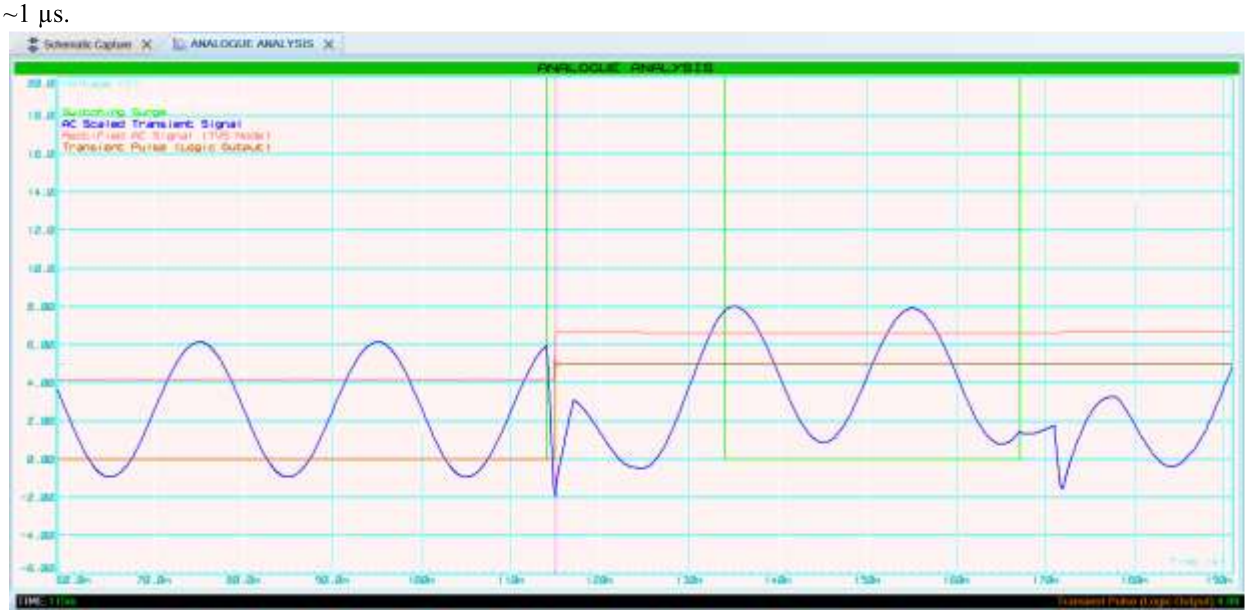
$$\Delta t = t_{interrupt} - t_{fault\text{-}onset} \quad (11)$$

The breakdown of hardware contributions to the delay is as follows:

Transformer/Magnetic Delay: Power transformers and inductive elements introduce a small delay due to magnetic flux buildup. This is usually in the hundreds of nanoseconds to a few microseconds range. Let's assume ~1 μs.

TVS Clamping Speed: SMBJ6.0A TVS diode activates extremely quickly, typically in the picosecond to nanosecond domain. A conservative value is ~1 ns.

Comparator Propagation Delay: The TLV2372D comparator datasheet specifies propagation delays in the hundreds of nanoseconds to a few microseconds, depending on input overdrive. A typical value is ~500 ns.



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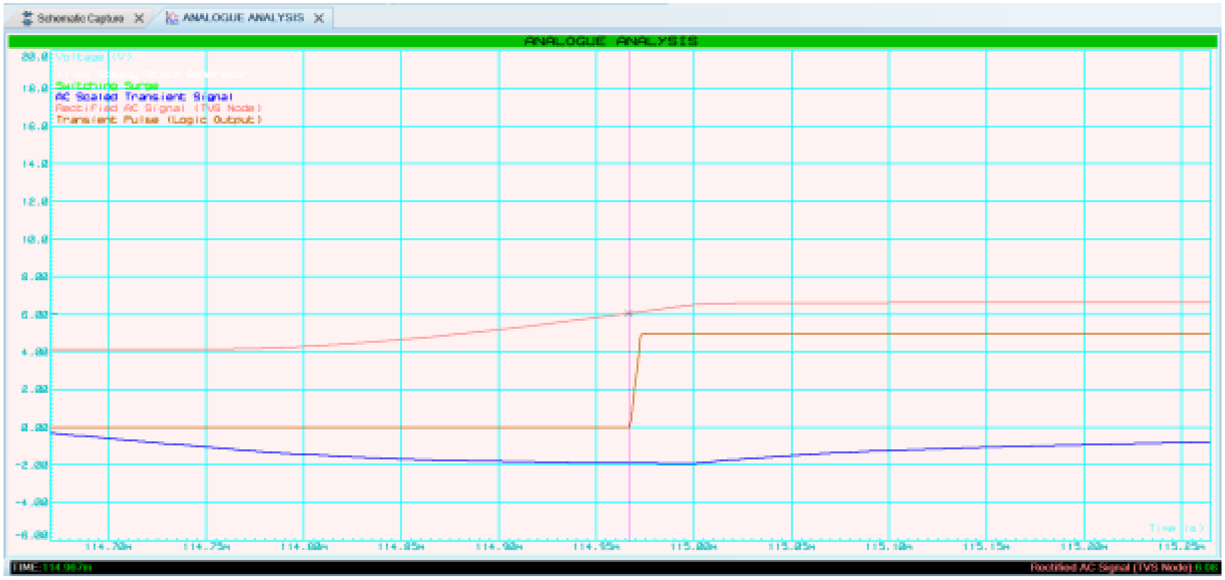

Figure 9: Simulated AC transient signal vs pulse output.

From the simulation graph of Figure 9, the $t_{fault\text{-}onset}$ started at 114.967 ms. while the $t_{interrupt}$ occurred at 114.976 ms. Therefore, the response time Δt is:

$\Delta t = 114.976 \text{ ms} - 114.96 \text{ ms} = 0.009 \text{ ms} = 9 \text{ µs}$

If microcontroller firmware integration is in the design, the interrupt pulse signal at 9 µs is fed to the microcontroller, which instantly pauses the microcontroller's main program loop to perform a trip action. The latency of MCUs are often 100 – 500 ns (0.1 - 0.5 μs). Therefore, the trip time is the addition of the MCU latency and the response time (Δt).

$$\text{Trip time} = \Delta t + \text{MCU Latency} \quad (12)$$

$$\text{Trip time} = 9 \text{ µs} + 0.5 \mu\text{s} = 9.5 \text{ µs}$$

V. CONCLUSION

The proposed detection technique demonstrates that a strictly linear, decoupled topology can reliably translate medium-voltage anomalies into low-voltage digital events with microsecond-level precision. By cascading transformer isolation, TVS diode clamping, and comparator thresholding, the system achieves a measured response latency of 9 µs, with theoretical hardware contributions in the sub-microsecond range. When integrated with microcontroller hardware interrupts, the additional MCU latency of 0.5 µs is negligible, yielding a total trip time of 9.5 µs. This validates the superiority of hardware-driven detection over software polling, ensuring ultra-fast, deterministic protection suitable for real-time breaker trip signaling in high-voltage environments.

VI. RECOMMENDATIONS

The study demonstrates that a TVS-diode-based detection technique can reliably translate medium-voltage anomalies into low-voltage digital events with microsecond-level precision. To strengthen the practical applicability of this approach, it is recommended that a scaled laboratory prototype be developed to validate simulation outcomes under real operating conditions. Further optimization of the comparator stage, particularly through the selection of devices with lower propagation delays, could reduce the overall trip time below 6 µs. Expanded transient testing, including lightning impulses, current chopping, and restrike events, is necessary to confirm robustness across diverse fault scenarios. Benchmarking different microcontroller families will also ensure consistency in interrupt latency and reinforce the superiority of hardware-driven detection over software polling.

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