© SEP 2026 | IRE Journals | Volume 10 Issue 3 | ISSN: 2456-8880
DOI: https://doi.org/10.64388/IREV10I3-1722747

Comparative Study and Performance Analysis of CMOS Ring-Oscillator Voltage-Controlled Oscillators

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Abstract- ***A voltage-controlled oscillator (VCO) is an important building block in phase-locked loops, frequency synthesizers, clock-generation circuits and wireless communication systems. A CMOS ring oscillator is attractive for integrated-circuit applications because it can be implemented without an on-chip inductor, occupies a small area and can provide a wide tuning range. This paper presents a comparative study of three-, five- and seven-stage CMOS ring-oscillator VCOs, with emphasis on oscillation frequency, propagation delay, power consumption and phase noise. The analytical relation between the number of delay stages and oscillation frequency is discussed, and published simulation/measurement results are used as a reference benchmark. The comparison shows the fundamental trade-off: adding inverter stages increases the total loop delay and therefore reduces oscillation frequency, while the additional stages can improve phase-noise performance. A published 180-nm CMOS study reported tuning ranges of 3.2909–4.2280 GHz, 1.9406–2.5769 GHz and 1.3984–1.8077 GHz for three-, five- and seven-stage ring VCOs, respectively, with corresponding power ranges of 335.4–486.2 μW, 559.0–810.3 μW and 782.6–1134.4 μW. These literature values are used only as benchmark data and are not claimed as new measurements in the present manuscript. The study indicates that a three-stage oscillator is preferable when high frequency is the primary requirement, whereas a five- or seven-stage design can be selected when phase noise, phase resolution and power-performance trade-offs are more important.***

Keywords: CMOS, Ring Oscillator, Voltage-Controlled Oscillator, VCO, Oscillation Frequency, Power Consumption, Propagation Delay, Phase Noise.

I. INTRODUCTION

A voltage-controlled oscillator is an oscillator whose instantaneous output frequency is controlled by an input tuning voltage. VCOs are widely used in phase-locked loops (PLLs), frequency synthesizers, clock generators, frequency modulation and wireless communication systems. In an ideal linearized model, the instantaneous frequency can be written as

$$f(t) = f_0 + K_v^{co}\, v^{tune}(t)$$

where f_0 is the free-running frequency, K_v^{co} is the VCO sensitivity in hertz per volt, and $v^{tune}(t)$ is the control voltage. The output phase is the time integral of the instantaneous angular frequency.

$$\varphi(t) = \varphi_0 + 2\pi \int_0^t f(\tau)d\tau$$

Among the different VCO architectures, the CMOS ring oscillator is especially suitable for highly integrated systems. It consists of an odd number of inverting delay stages connected in a closed loop. The odd inversion count prevents a stable DC state and, together with the propagation delay of the stages, produces periodic oscillation. Unlike LC oscillators, a ring oscillator does not require a large on-chip spiral inductor, which makes it attractive where silicon area and implementation simplicity are important.

Earlier work has demonstrated measured three-stage ring-VCO operation in 180-nm CMOS over a wide frequency range. Other published work has compared three-, five- and seven-stage VCOs and reported a clear decrease in frequency and an increase in power with increasing stage count, while phase-noise performance improved with additional stages. Recent work has further shown the importance of technology scaling and systematic comparison of frequency, power, delay and phase noise.

II. CMOS RING OSCILLATOR VCO

A basic CMOS ring oscillator is formed by connecting the output of the last inverter to the input of the first inverter. For sustained oscillation, the number of inverting stages N must be odd. If the propagation delay of each stage is approximately t_d, the total transition delay around the loop is approximately 2Nt_d. Hence the fundamental oscillation frequency is

$f_{os}c \approx 1 / (2 N t\_d)$

This expression shows directly why increasing the number of stages lowers the oscillation frequency when the individual stage delay is kept approximately constant. In a practical VCO, the control voltage changes the effective charging/discharging current and therefore the delay of each stage. Consequently, the tuning voltage changes t_d and hence $f_{os}c$.

III. CLASSIFICATION OF VCOS

VCOs can broadly be grouped into waveform/relaxation oscillators and resonant oscillators. Waveform VCOs commonly generate square, triangular or sawtooth waveforms and are convenient for monolithic implementation. Ring oscillators belong to this group. Resonant VCOs, such as LC-tank and crystal-based oscillators, generate more sinusoidal signals and are generally preferred when very low phase noise and high frequency stability are required.

3.1 Ring-Oscillator VCO

- Uses an odd number of CMOS inverter/delay stages connected in a closed loop.
- The control voltage changes the effective delay of each stage and therefore tunes the oscillation frequency.
- Offers compact implementation and does not require a large integrated inductor.
- Provides multiple phase outputs, which can be useful in clocking, timing and communication circuits.

3.2 Resonant VCO

- Uses an LC tank or another resonant element to determine the oscillation frequency.
- A varactor can be used to make the resonant frequency voltage-controlled.
- Generally provides better phase-noise performance than a basic ring oscillator, but often requires larger area and more complex integrated passive components.

IV. PERFORMANCE PARAMETERS

- Oscillation frequency: the output frequency and an indicator of speed.
- Frequency tuning range: the range of frequencies obtained over the specified control-voltage range.
- Power consumption: the electrical power required by the oscillator; dynamic power is strongly related to switching activity and capacitance.
- Propagation delay: the delay introduced by each inverter stage; it is a major factor controlling ring-oscillator frequency.
- Phase noise: short-term spectral instability of the oscillator, normally expressed in dBc/Hz at a specified frequency offset.
- Figure of Merit (FoM): a normalized metric that can be used to compare oscillator designs under different operating conditions.

V. COMPARATIVE ANALYSIS OF 3-, 5- AND 7-STAGE RING VCOS

The present comparison focuses on the effect of stage count. The original manuscript used qualitative labels such as high, medium and low. For publication, it is preferable to distinguish clearly between analytical conclusions and measured/simulated data. Therefore, the numerical values below are identified as published benchmark data from a 180-nm CMOS study rather than as new results generated by this work.

Design	Frequency range (GHz)	VDD (V)	Technology	Power range	Phase noise @ 1 MHz
3-stage	3.2909–4.2280	1.8	0.18 µm	335.4–486.2 µW	−80.95 dBc/Hz
5-stage	1.9406–2.5769	1.8	0.18 µm	559.0–810.3 µW	−84.56 dBc/Hz
7-stage	1.3984–1.8077	1.8	0.18 µm	782.6–1134.4 µW	−86.65 dBc/Hz

Table 1 shows the expected trend in the published benchmark: the three-stage design provides the highest frequency range and the lowest power range among the three reported configurations, while the seven-stage design provides the lowest frequency range and the highest power range. Phase noise becomes more negative as the stage count increases, indicating improved phase-noise performance in that particular implementation. Because these values belong to a published design, they should not be presented as original experimental results of the present paper unless the same circuits are independently reproduced and simulated.

VI. EFFECT OF NUMBER OF STAGES

6.1 Effect on Oscillation Frequency

From $f_{osc} \approx 1/(2Nt\_d)$, the oscillation frequency is approximately inversely proportional to the number of stages for comparable stage delay. Thus, a three-stage ring oscillator generally operates faster than five- and seven-stage versions. This relationship is also visible in the published 180-nm benchmark data.

6.2 Effect on Power Consumption

Adding stages increases the number of switching nodes and therefore tends to increase the total capacitive switching activity. At the same supply voltage and comparable device conditions, this can increase power consumption. However, actual power depends on transistor sizing, load capacitance, frequency, biasing and technology-node leakage, so power should always be reported from a defined simulation or measurement condition.

6.3 Effect on Phase Noise

Phase noise is influenced by device noise, waveform slope, delay-cell design, supply noise and the number of stages. Published results for three-, five- and seven-stage ring VCOs show progressively improved phase-noise figures at a 1-MHz offset in one 180-nm implementation. This should be interpreted as a design-specific result rather than a universal rule; phase-noise behavior can change with architecture, biasing and technology.

6.4 Propagation Delay

Propagation delay is the principal timing quantity controlling a ring oscillator. For approximately identical stages, increasing N increases the total loop delay and reduces frequency. Device dimensions, fan-out, load capacitance and supply voltage all influence the delay and must be kept consistent when making a fair comparison.

VII. METHODOLOGY FOR AN ORIGINAL SIMULATION STUDY

To convert this comparative manuscript into a fully original simulation paper, the three oscillator topologies should be implemented using the same CMOS technology, supply voltage, load capacitance, transistor sizing strategy and control-voltage range.

The following procedure is recommended:

- Design identical 3-stage, 5-stage and 7-stage CMOS ring oscillators.
- Use the same technology model and supply-voltage condition for all three designs.
- Sweep the control voltage over a clearly stated range and record the steady-state oscillation frequency.
- Measure the propagation delay of an individual delay cell and verify the analytical relation $f_{osc} \approx 1/(2Nt\_d)$.
- Measure average power over a steady-state interval using the same load conditions.
- Perform phase-noise analysis at a specified offset, such as 1 MHz, using the same simulator settings.
- Report the exact simulator, technology node, transistor dimensions, supply voltage, load, control-voltage range and measurement conditions.

- Repeat simulations, where possible, over process, voltage and temperature corners to assess robustness.

Until such simulation data are available, the manuscript should describe the numerical table as a literature benchmark and should not label it as 'present simulation results'.

VIII. DISCUSSION

The comparison demonstrates a fundamental architecture trade-off. A smaller number of stages reduces the total loop delay and is therefore advantageous for high-speed operation. More stages increase the delay and generally reduce frequency, but they can provide more phase outputs and may improve phase-noise performance in suitable delay-cell architectures. The best topology therefore depends on the target application. High-speed clock generation may favor a three-stage structure, whereas applications requiring more phases or improved spectral purity may favor five- or seven-stage structures.

Recent comparative research has also shown that technology scaling can substantially change frequency, power and leakage behavior. For example, a 2026 study comparing 45-nm and 180-nm five- and seven-stage oscillators reported 1.25 GHz/2.95 mW for a 45-nm five-stage design and 0.892 GHz/2.31 mW for a 45-nm seven-stage design under its specified simulation conditions. Such results reinforce the need to state technology node and simulation conditions whenever oscillator performance is compared.

IX. BENCHMARK FIGURES AND RESULTS

The following figures visualize the published 180-nm CMOS benchmark values reported in the literature and already tabulated in this manuscript. They are included to improve readability and should be labeled as literature benchmarks, not as original simulations by the present authors.

Figure 1. Conceptual CMOS ring-oscillator structure

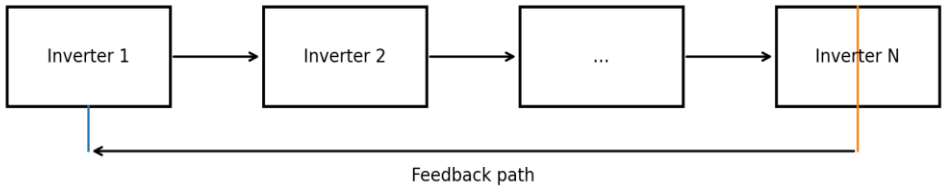

Figure 5. Conceptual CMOS ring-oscillator structure. The feedback path connects the output of the final inverter to the input of the first inverter.

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DOI: https://doi.org/10.64388/IREV10I3-1722747

Figure 2. Published benchmark frequency ranges

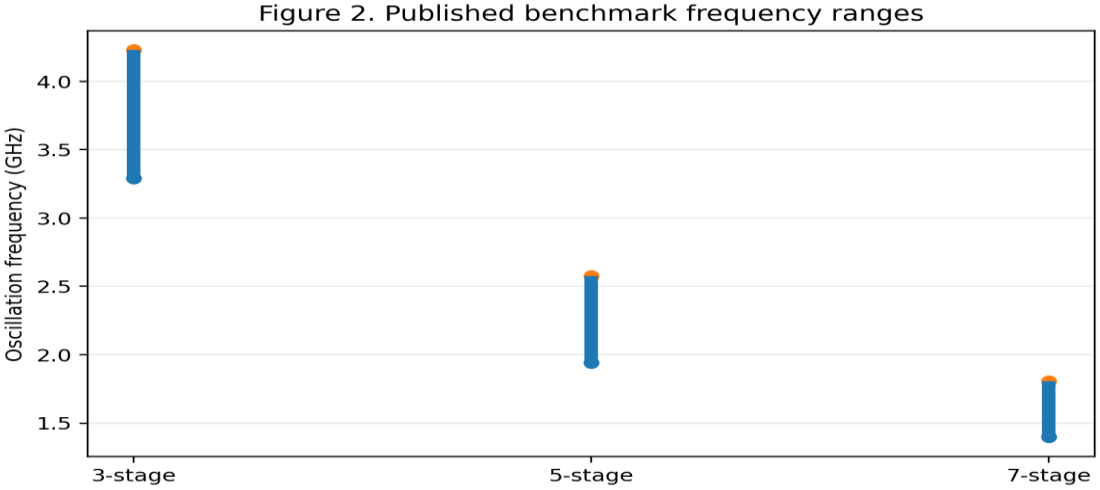

Figure 6. Published benchmark oscillation-frequency ranges for 3-, 5- and 7-stage ring VCOs.

Figure 3. Published benchmark power ranges

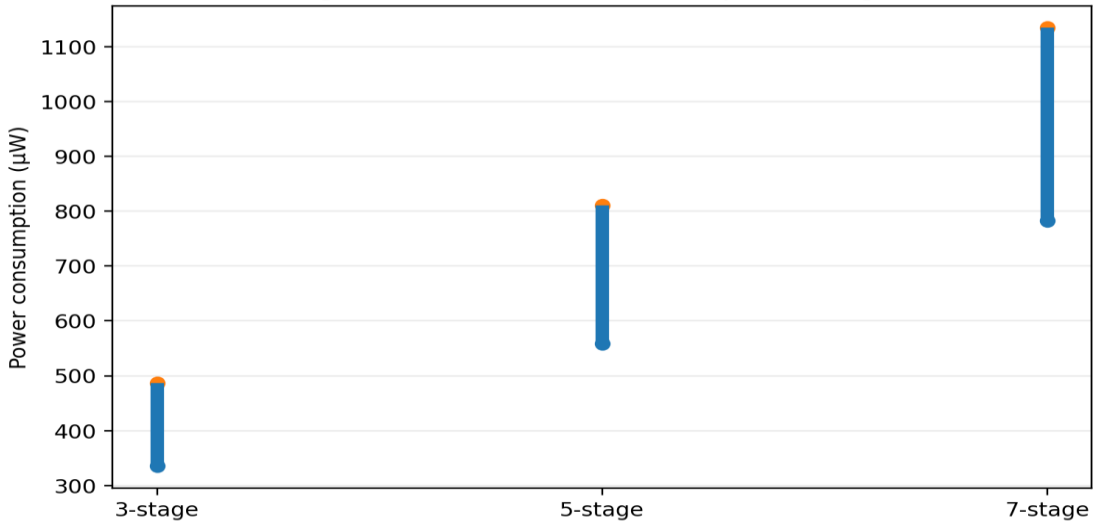

Figure 7. Published benchmark power-consumption ranges for 3-, 5- and 7-stage ring VCOs.

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DOI: https://doi.org/10.64388/IREV10I3-1722747

Figure 4. Published benchmark phase-noise values

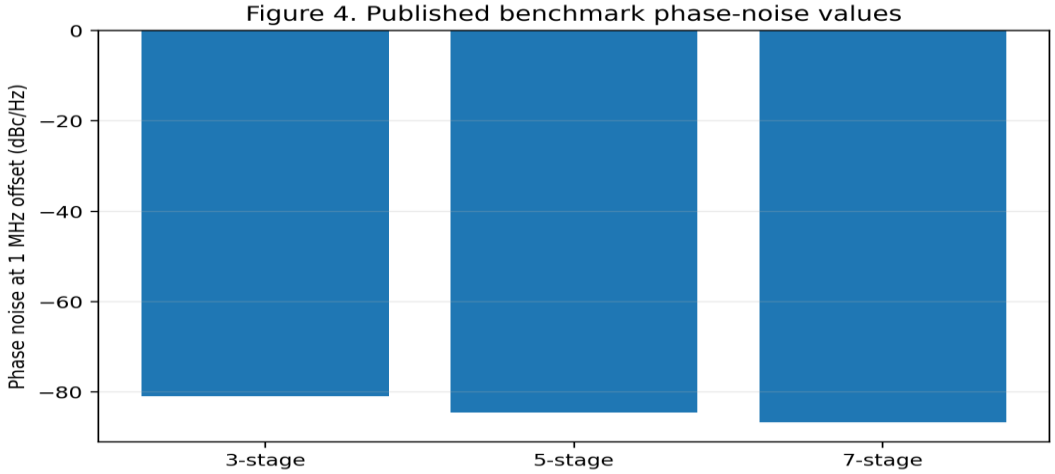

Figure 8. Published benchmark phase-noise values at 1-MHz offset.

Note: Figures 6–8 are plotted from published benchmark values. To claim original simulation performance, the same designs must be independently simulated under explicitly stated technology, supply, sizing, load and control-voltage conditions.

X. APPLICATIONS

- Phase-locked loops (PLLs)
- Frequency synthesizers
- Clock generation and clock recovery
- Wireless communication systems
- Digital and mixed-signal integrated circuits
- Microprocessors and embedded systems
- Multi-phase timing and clocking circuits
- Internet-of-Things (IoT) devices

XI. CONCLUSION

This paper presented a comparative analysis of three-, five- and seven-stage CMOS ring-oscillator VCOs. The analytical model shows that oscillation frequency decreases as the number of stages increases because the total loop delay increases. Published 180-nm CMOS benchmark results also demonstrate this frequency trend and show that power and phase-noise performance depend strongly on stage count and circuit implementation. A three-stage topology is attractive for high-frequency operation, while five- and seven-stage topologies can be considered when additional phase outputs and improved phase-noise performance are important. For a strong original research publication, the next essential step is to provide reproducible simulation or measurement results using a specified CMOS technology, control-voltage range, supply voltage, transistor sizing and simulator. Such results will allow the manuscript to move from a qualitative/literature-based comparison to a verifiable original performance analysis.

REFERENCES

[1] Godse, A. P., & Bakshi, U. A. (2009). *Linear Integrated Circuits and Applications.* Technical Publications.

[2] Salivahanan, S. (2008). *Linear Integrated Circuits.* Tata McGraw-Hill Education.

[3] Kumar, S., et al. (2013). A Low Power Voltage Controlled Oscillator Design. *International Scholarly Research Notices, 2013*, Article 987179. https://doi.org/10.1155/2013/987179.

[4] Design and analysis of a three-stage voltage-controlled ring oscillator. *Journal of Semiconductors, 34*(11), 115003. https://doi.org/10.1088/1674-4926/34/11/115003.

[5] Andreani, P., & Bevilacqua, A. (2021). Harmonic Oscillators in CMOS—A Tutorial Overview. *IEEE Open Journal of the Solid-State Circuits Society, 1*, 2–17.

https://doi.org/10.1109/OJSSCS.2021.3109854.

[6] Shiva, K., & Hemantha, R. G. (2026). Design, simulation, and cross-technology comparative analysis of 5-stage and 7-stage CMOS ring oscillators with machine learning-assisted performance prediction and PSO-based power optimisation. *Journal of Engineering and Applied Science, 73*(1). https://doi.org/10.1186/s44147-026-00996-7.

[7] Rhea, R. W. (1997). *Oscillator Design & Computer Simulation* (2nd ed.). McGraw-Hill.

[8] Thomas, D. E. (1954). Single-Transistor F-M Transmitter. *Electronics, 27*(2), 130–133.