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Effect of Gate Length Scaling on the Electrical Characteristics of a Ge/Si Double-Gate Heterojunction TFET

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Abstract

This paper investigates the effect of gate-length scaling on the electrical characteristics and band-to-band tunneling behavior of a Ge/Si double-gate heterojunction tunnel field-effect transistor (TFET) using Silvaco ATLAS TCAD. Twelve gate lengths ranging from 1 to 20 nm are simulated while the principal device geometry, doping concentrations, gate dielectric thickness, and gate work function are kept constant. The electrical performance is evaluated in terms of ON-state current, OFF-state current, ON/OFF current ratio, threshold voltage, point subthreshold swing, and peak transconductance. The results show that the ON-state current increases from 9.99×10^{-9} to 1.51×10^{-4} A as gate length increases from 1 to 20 nm, while the ON/OFF current ratio reaches 1.08×10^{11}. The extracted threshold voltage decreases from 1.24 to 0.46 V, and the point subthreshold swing decreases from 23.42 to 10.00 mV/dec. Peak transconductance reaches 1.63×10^{-3} S at a gate length of 19 nm before decreasing slightly at 20 nm. Energy-band, electric-field, and nonlocal band-to-band tunneling generation profiles are also examined to support the interpretation of the electrical trends. These findings demonstrate the influence of gate length on the simulated electrical performance and tunneling behavior of the investigated Ge/Si double-gate heterojunction TFET.

Keywords: tunnel field-effect transistor (TFET); Ge/Si heterojunction; double-gate transistor; gate-length scaling; Silvaco ATLAS; band-to-band tunneling

1 Introduction

The continued scaling of conventional MOSFETs has increased challenges related to leakage current, short-channel effects, and power consumption, motivating the development of alternative low-power switching devices. Tunnel field-effect transistors (TFETs) utilize band-to-band tunneling (BTBT) rather than thermionic emission as the dominant switching mechanism and can provide low OFF-state current and steep subthreshold characteristics. Double-gate (DG) architectures further improve electrostatic control over the channel and tunneling junction. However, the scaling behavior of TFETs differs from that of conventional MOSFETs, and the influence of device dimensions on tunneling and switching characteristics must therefore be carefully evaluated [1].

Heterojunction engineering provides an approach for improving TFET performance by modifying the tunneling barrier and band alignment. Toh et al. demonstrated the importance of SiGe/Si heterojunction positioning in a double-gate TFET and showed that appropriate alignment can enhance band-to-

band tunneling (BTBT) [2]. Ge–Si heterojunction TFETs have also been investigated using nanowire structures, with emphasis on tunneling characteristics and BTBT modeling [3].

In addition, Silvaco ATLAS-based simulation studies have compared single-gate and double-gate TFETs and investigated the influence of gate length, gate work function, and intrinsic-layer thickness on subthreshold swing and the I_{ON}/I_{OFF} ratio [4]. Further studies have explored SiGe/Si heterojunction double-gate TFETs using heterogeneous gate dielectrics and additional structural engineering to improve switching performance [5].

Gate-length scaling has also been investigated in TFETs. Boucart and Ionescu analyzed the influence of gate length on parameters including threshold voltage, subthreshold swing, I_{ON}, I_{OFF}, and transconductance in double-gate TFETs [1]. Ge–Si heterojunction nanowire TFETs have also been examined for the effects of gate length and nanowire diameter on subthreshold swing [3]. In addition, gate-length and drain-voltage effects have been investigated in asymmetric double-gate doping-less Si/Ge heterojunction TFETs [6]. Recent work on Ge-source DG-TFETs has also explored strain and channel engineering to improve DC and high-frequency performance [7]. Although gate-length effects have therefore been examined in several TFET configurations, differences in device architecture and the simultaneous use of other structural or material engineering approaches make direct comparison difficult. This motivates a systematic assessment of gate-length dependence in the Ge/Si double-gate TFET configuration considered in this work, with the principal device parameters kept fixed and the electrical trends correlated with tunneling-related physical quantities.

In this work, the effect of varying the gate length from 1 to 20 nm on a Ge/Si double-gate heterojunction TFET is investigated using Silvaco ATLAS. The source, channel, and drain dimensions, doping concentrations, HfO_2 gate dielectric thickness, and gate work function are kept fixed while twelve gate-length conditions are evaluated. The resulting changes in I_{ON}, I_{OFF} , I_{ON}/I_{OFF}, threshold voltage, subthreshold swing, and peak transconductance are analyzed. To understand the physical origin of the observed electrical trends, gate-length-dependent energy-band, electric-field, and nonlocal BTBT generation profiles are also examined. The study provides a systematic assessment of the influence of gate length on the electrical characteristics and tunneling behavior of the Ge/Si double-gate heterojunction TFET.

2 Device structure and simulation methodology

2.1 Device structure and material configuration

The simulated device is a two-dimensional double-gate heterojunction tunnel field-effect transistor (TFET) consisting of a Ge source, Si channel, and Si drain (Figure 1). The total semiconductor length is 65 nm, comprising source, channel, and drain lengths of 22.5, 20, and 22.5 nm, respectively. The semiconductor body thickness is 5 nm. The Ge source is p-type doped at 1×10^{20} cm^{-3}, while the Si channel and drain are n-type doped at 1×10^{17} cm^{-3} and 5×10^{18} cm^{-3}, respectively. The Ge/Si source-channel interface forms the heterojunction responsible for the tunneling process. Two gate electrodes are positioned on opposite sides of the semiconductor body and are electrically connected to a common gate terminal. HfO_2 is used as the gate dielectric with a physical thickness of 2 nm, and the gate work function is set to 4.5 eV. These structural and material parameters are maintained constant throughout the gate-length scaling study.

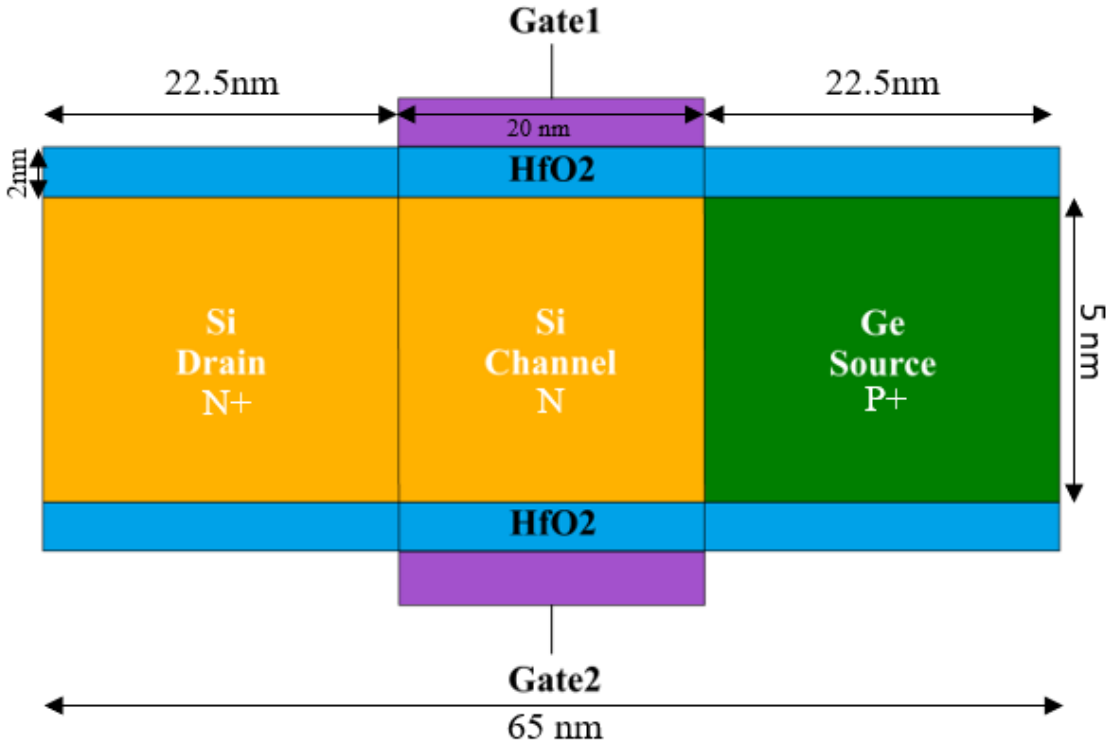


Figure 1. Ge/Si DG-H-TFET device structure.

2.2 Gate-length scaling strategy

The gate length L_G is the primary variable investigated in this work. Twelve gate-length values of 1, 3, 5, 7, 9, 10, 11, 13, 15, 17, 19, and 20 nm are considered. The source, channel, and drain dimensions, semiconductor materials, doping concentrations, HfO_2 thickness, gate work function, physical models, bias conditions, and extraction procedures are kept unchanged for all cases. Thus, the comparative analysis isolates the influence of gate-length variation on the device characteristics. This controlled scaling approach allows the effect of gate length to be evaluated through the variation of I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, threshold voltage, subthreshold swing, and transconductance.

2.3 TCAD simulation and physical models

The device is simulated using the two-dimensional Silvaco ATLAS TCAD simulator. The device geometry, material regions, doping profiles, electrodes, mesh, physical models, and bias conditions are defined in the simulation deck. The mesh is refined around the material interfaces and junction regions to adequately represent the spatial variation of the device quantities.

The nonlocal band-to-band tunneling model (BBT.NONLOCAL) is employed to model the tunneling process, with BBT.FORWARD and QTUNN.DIR=1 used to configure the tunneling calculation. The bandgap-narrowing (BGN) model is included to account for high-doping effects, while Shockley–Read–Hall recombination (CONSRH) and concentration-dependent mobility (CONMOB) are included for carrier recombination and transport effects, respectively. The same physical-model configuration is used for all gate-length cases to maintain a consistent comparison.

2.4 Bias conditions and electrical parameter extraction

After device initialization, the transfer characteristics are obtained by sweeping the common gate voltage from 0 to 1.5 V in steps of 0.02 V at a fixed drain-to-source voltage of V_{DS} = 1.0 V. The drain current I_D is recorded as a function of gate voltage for each of the twelve gate-length cases. The same bias condition and extraction procedures are applied to all cases for consistent comparison.

The extracted parameters are I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, V_{TH}, point subthreshold swing (SS), average subthreshold swing (SS_{AVG}), and transconductance (g_m) are obtained from the simulated transfer characteristics under the selected ON-state and OFF-state conditions, while the I_{ON}/I_{OFF} ratio is calculated from the corresponding current values. The threshold voltage is extracted using a drain-current criterion of 10^{-7} A, applied consistently to all gate lengths.

The point subthreshold swing is evaluated from the logarithmic transfer characteristic as.

$$SS = \frac{dV_{GS}}{d(\log_{10}|I_D|)} \tag{1}$$

and expressed in mV/dec. In this work, the point SS is obtained using the maximum-slope extraction procedure specified in the ATLAS deck. The average subthreshold swing is obtained using the extraction procedure defined in the simulation deck over the selected current interval.

The transconductance is calculated as.

$$g_m = \frac{dI_D}{dV_{GS}} \tag{2}$$

at fixed drain voltage. The extracted electrical parameters are then compared as a function of gate length to identify the scaling-dependent trends.

3 Results and discussion

3.1 Transfer characteristics and drain current

The transfer characteristics of the device for the twelve gate lengths are shown in Figure 2.

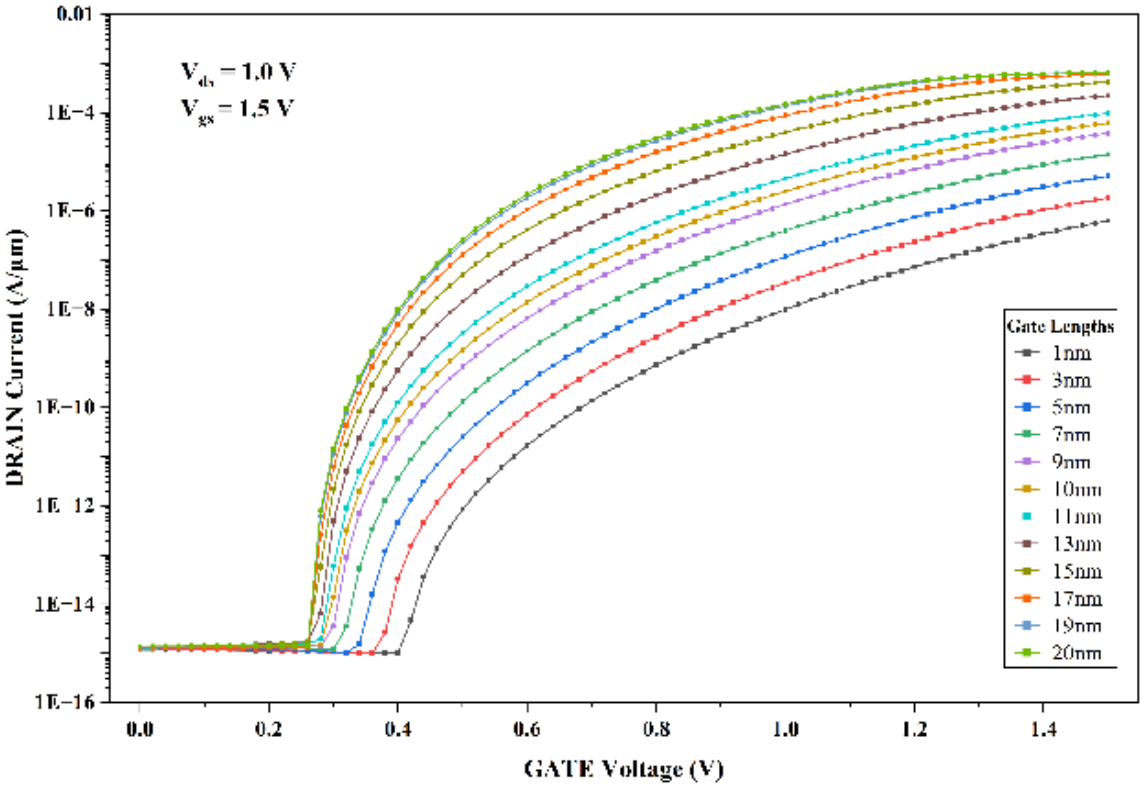


Figure 2. Transfer characteristics of the proposed device.

The ON-state drain current I_{ON} is evaluated at V_{GS} = 1.0 V, with the drain-to-source voltage maintained at V_{DS} = 1.0 V. The extracted I_{ON} increases from 9.99×10^{-9} A at 1 nm to 1.51×10^{-4} A at 20 nm. In comparison, the OFF-state current changes only slightly, from 1.16×10^{-15} A to 1.39×10^{-15} A over the same gate-length range (Figure 3).

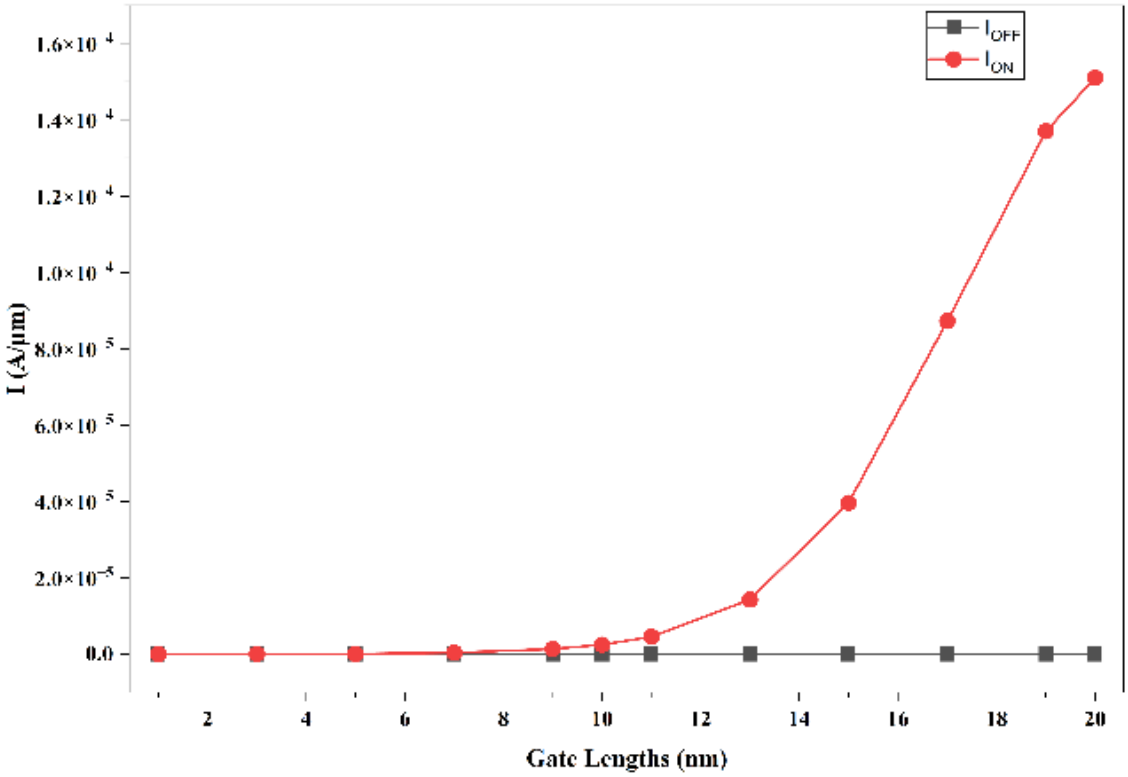


Figure 3. Variation of I_{ON} and I_{OFF} with gate length.

The much larger variation in I_{ON} compared with I_{OFF} results in a strong improvement in the I_{ON}/I_{OFF} ratio. The ratio increases from 8.61×10^{6} at a gate length of 1 nm to 1.08×10^{11} at 20 nm (Figure 4).

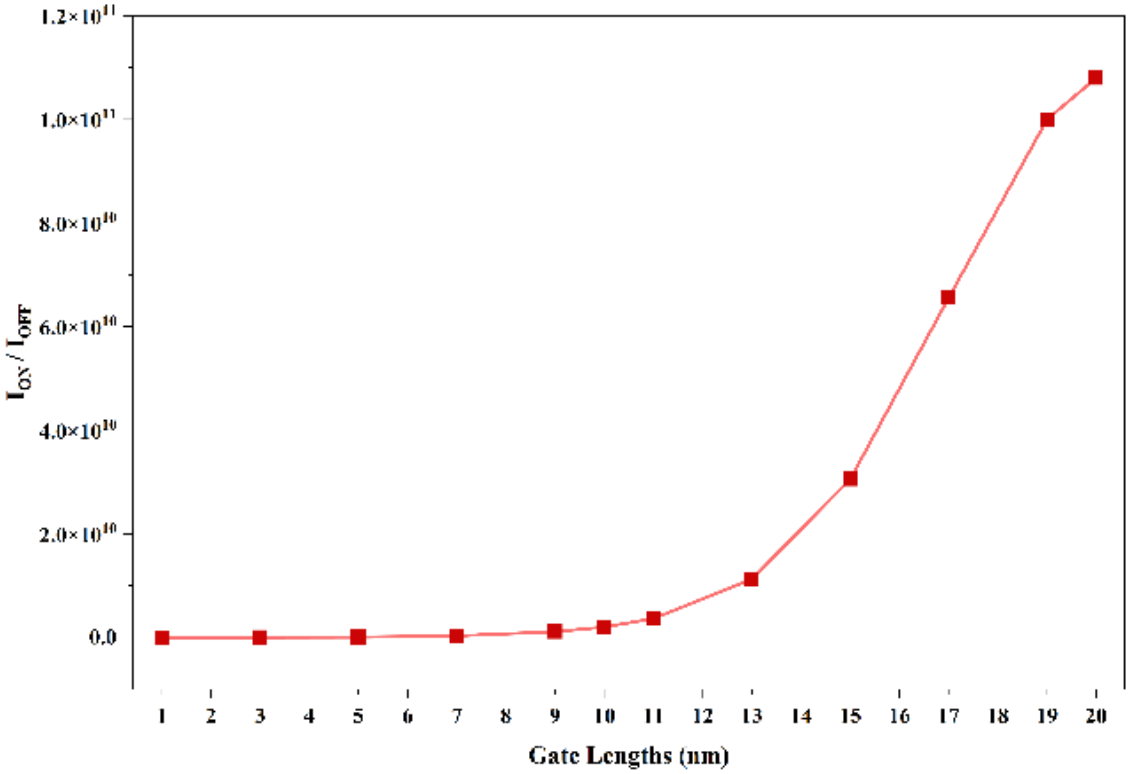


Figure 4. Variation of the I_{ON}/I_{OFF} current ratio with gate length.

Since the source, channel, and drain dimensions and the other device parameters are maintained constant, the observed differences in the transfer characteristics are primarily associated with the variation in gate length. The results therefore demonstrate a strong dependence of the simulated current characteristics on gate length in the investigated Ge/Si double-gate heterojunction TFET.

3.2 Threshold voltage and point subthreshold swing

Threshold voltage (V_{TH}) and point subthreshold swing (SS_{Point}) are used to evaluate the switching characteristics of the Ge/Si double-gate heterojunction TFET. As the gate length increases from 1 to 20 nm, the extracted threshold voltage decreases from 1.24 V to 0.46 V (Figure 5). Threshold voltage (V_{TH}) was estimated from the simulated transfer characteristics using the drain-current criterion of I_D at 10^{-7} A. The corresponding gate voltage was identified using the cursor in TonyPlot for each gate length.

The point subthreshold swing decreases from 23.42 mV/dec at a gate length of 1 nm to 10.00 mV/dec at 20 nm (Figure 6). The point subthreshold swing (SS) is calculated using the maximum derivative of the logarithmic drain current with respect to gate voltage, as implemented in the ATLAS extraction expression. The extracted values are converted to mV/dec and compared across the twelve gate lengths.

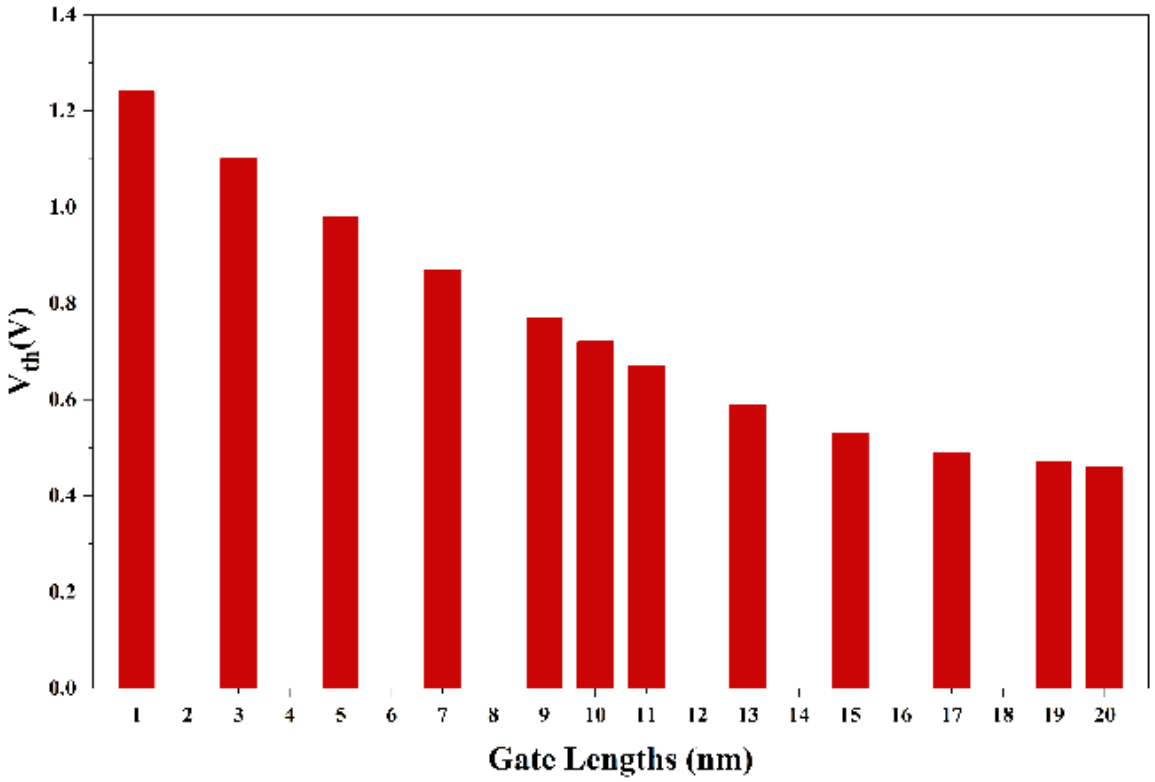


Figure 5. Variation of threshold voltage with gate length.

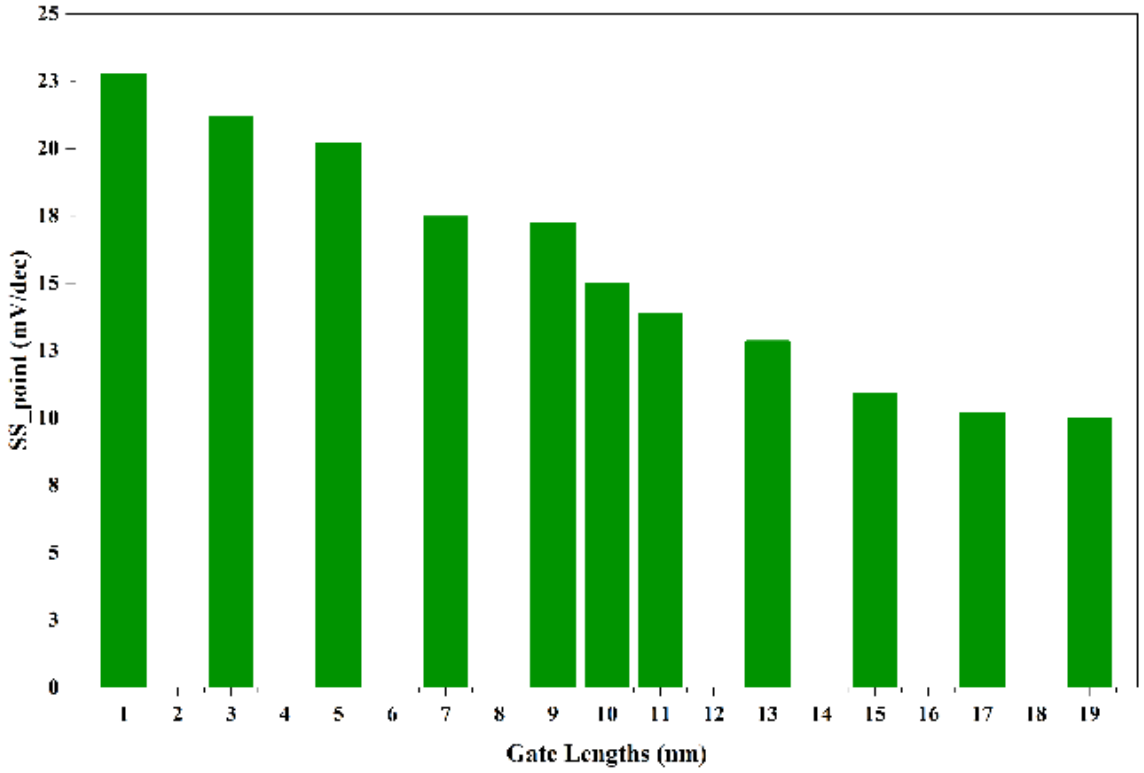


Figure 6. Variation of point subthreshold swing with gate length.

3.3 Transconductance analysis

Transconductance (g_m) describes the change in drain current with respect to gate voltage at a fixed drain-to-source voltage. It is an important parameter for evaluating the gate-control capability of the TFET.

The simulated results show that peak transconductance increases significantly as the gate length increases from 1 to 19 nm (Figure 7). It rises from 3.32×10^{-6} S at 1 nm to a maximum of 1.63×10^{-3} S at 19 nm. When the gate length increases further to 20 nm, the peak transconductance decreases slightly to 1.60×10^{-3} S. Therefore, 19 nm provides the highest peak transconductance among the twelve simulated gate-length conditions.

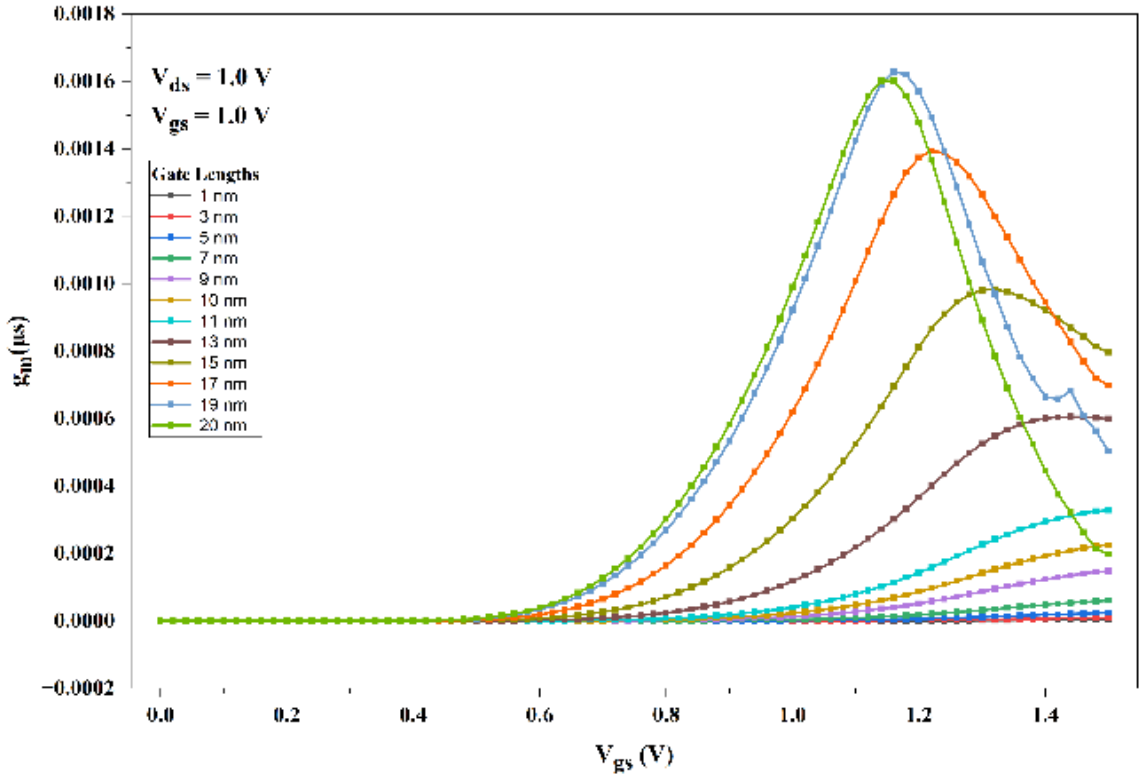


Figure 7. Variation of peak transconductance with gate length.

The overall increase in peak transconductance indicates a stronger change in drain current with gate voltage for the longer gate-length cases under the simulated conditions. However, the slight reduction at 20 nm shows that the peak transconductance does not increase monotonically over the entire investigated range. This result also demonstrates that the gate length giving the highest transconductance is not necessarily the same as the gate length giving the highest ON-current or ON/OFF current ratio.

3.4 Tunneling and electrostatic behavior

The energy-band profiles are examined under equilibrium, OFF-state, and ON-state conditions to understand the tunneling behavior of the Ge/Si double-gate heterojunction TFET. At equilibrium, the band alignment at the Ge source–Si channel heterojunction indicates the energy barrier associated with carrier injection (Figure 8).

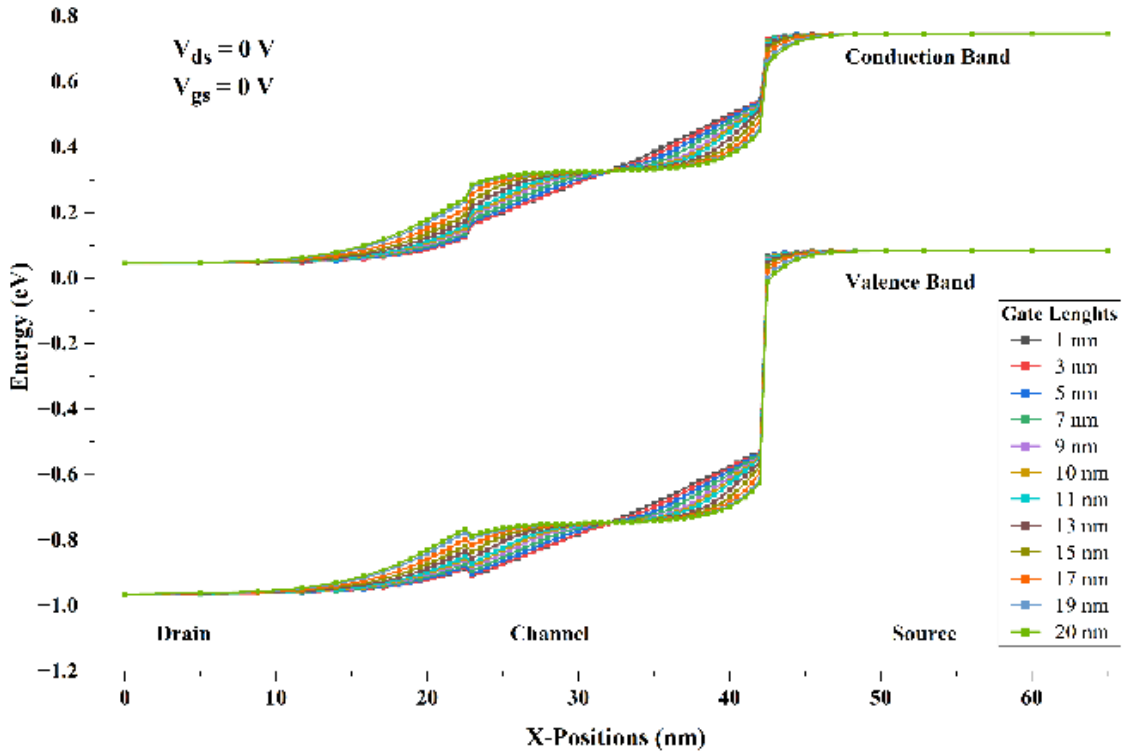


Figure 8. Energy band profiles under equilibrium.

Under OFF-state conditions, the applied bias modifies the band profile, while the tunneling barrier continues to influence carrier transport (Figure 9).

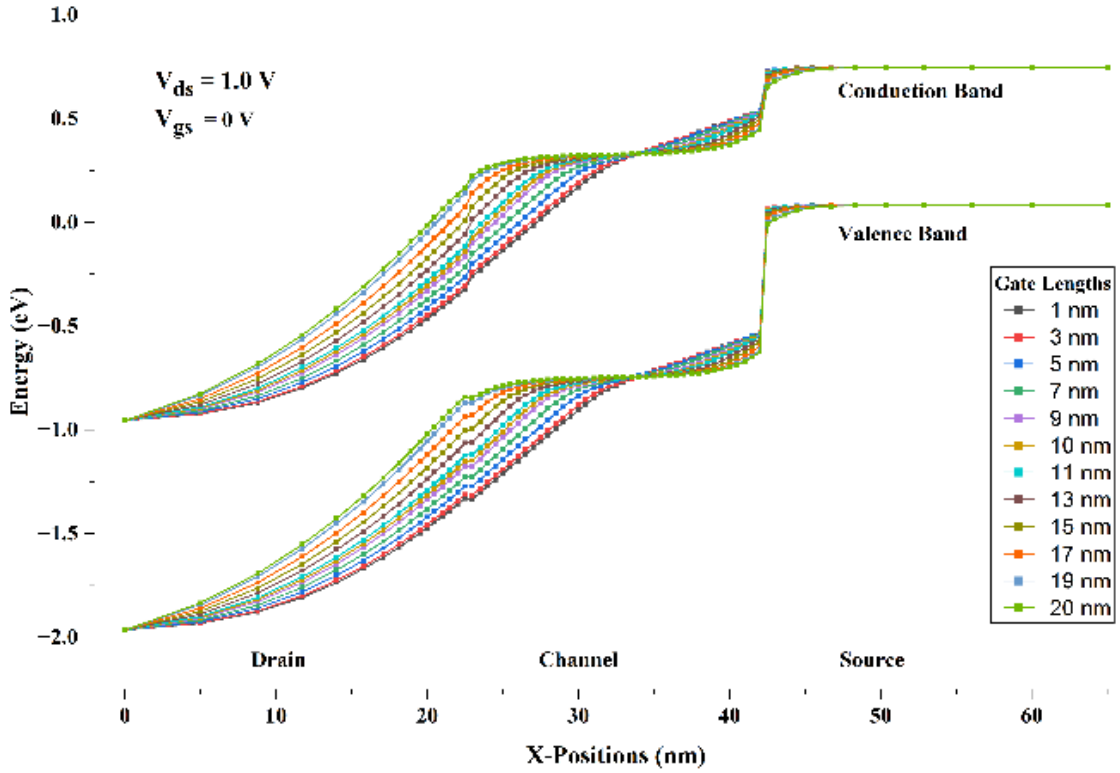


Figure 9. Energy band profiles under OFF-state.

Under ON-state conditions, the gate bias changes the band alignment near the source–channel interface, influencing the conditions for band-to-band tunneling (BTBT) (Figure 10). These profiles provide a physical basis for interpreting the current variation observed in the transfer characteristics.

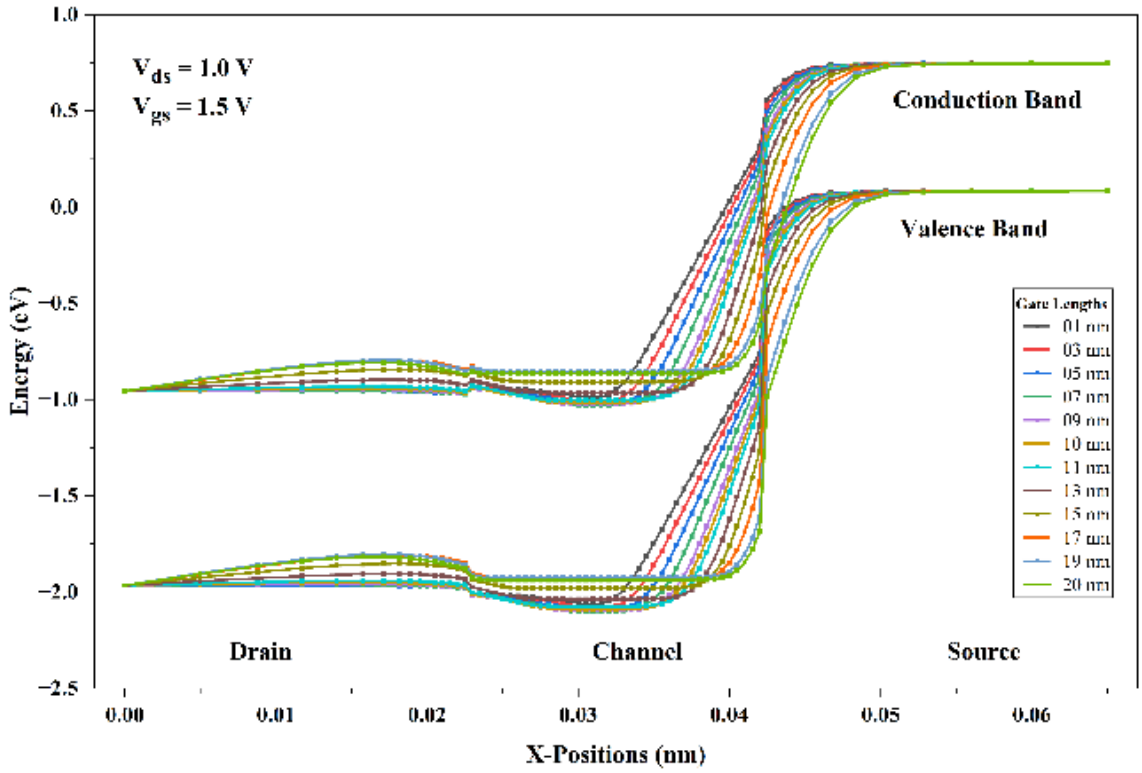


Figure 10. Energy band profiles under ON-state.

The electric-field distribution and nonlocal BTBT-generation profiles provide additional information about the spatial characteristics of the tunneling process (Figures 11 and 12). The electric field influences the band bending near the source–channel heterojunction, while the BTBT-generation profile identifies the region in which tunneling-related carrier generation occurs. Examining these profiles together helps relate the internal field distribution and tunneling behavior to the simulated drain-current characteristics.

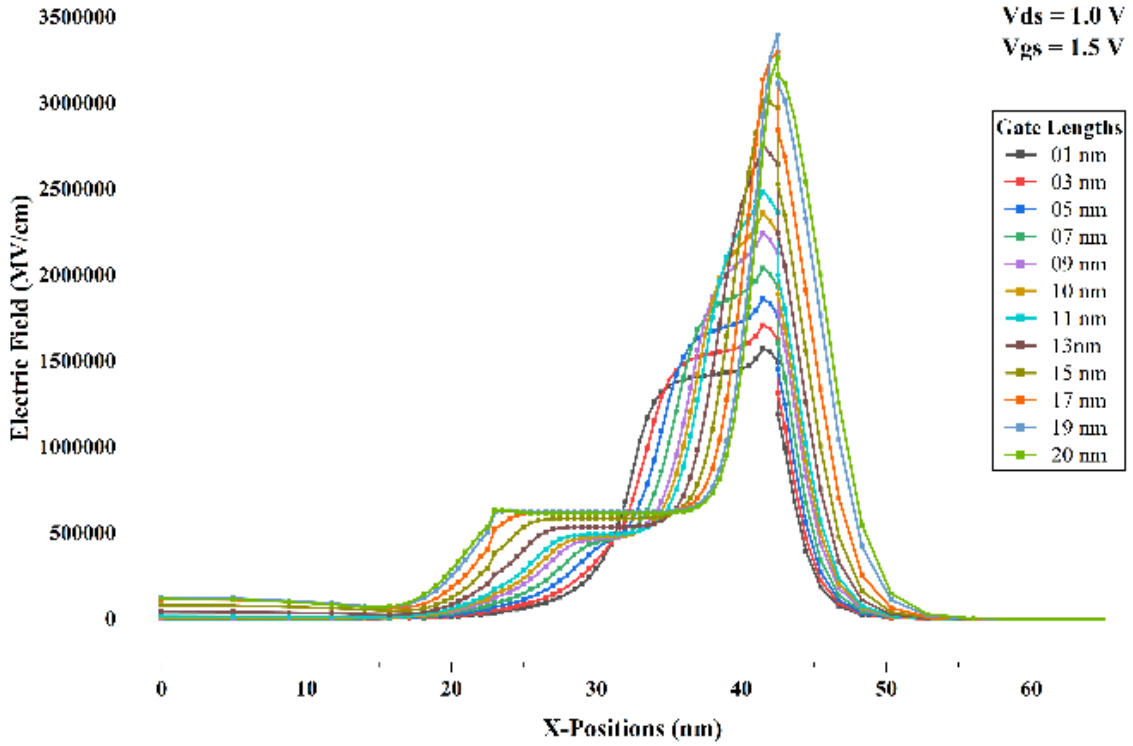


Figure 11. Electric field distribution.

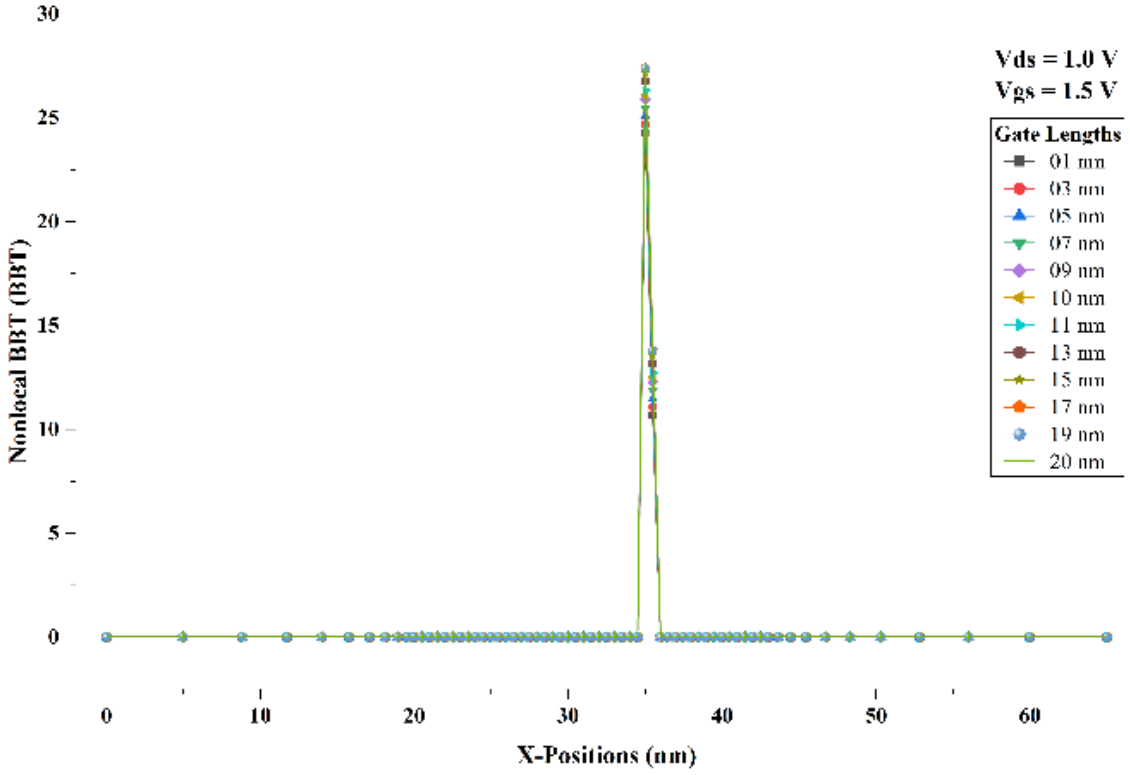


Figure 12. Nonlocal band-to-band tunneling generation profile.

The carrier-concentration and electrostatic-potential profiles provide further insight into the internal distribution of carriers and potential within the device. Together, these physical results complement the electrical analysis and help explain how gate-length variation affects the simulated operation of the Ge/Si double-gate heterojunction TFET.

4 Conclusion

The gate-length scaling characteristics of a Ge/Si double-gate heterojunction TFET were investigated using Silvaco ATLAS for twelve gate lengths ranging from 1 to 20 nm. The results show that the ON-state current and ON/OFF current ratio increase significantly with gate length, while the extracted threshold voltage and point subthreshold swing decrease.

The ON-state current increases from 9.99×10^{-9} A to 1.51×10^{-4}A, and the ON/OFF current ratio reaches 1.08×10^{11} at 20 nm. The extracted point subthreshold swing decreases from 23.42 to 10.00 mV/dec. Peak transconductance reaches a maximum of 1.63×10^{-3} S at 19 nm before decreasing slightly at 20 nm.

The energy-band, electric-field, and nonlocal band-to-band tunneling profiles provide additional insight into the physical behavior associated with gate-length variation. Overall, the results demonstrate that gate length significantly influences the electrical characteristics and tunneling behavior of the investigated device. The preferred gate length therefore depends on the performance parameter being prioritized.

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